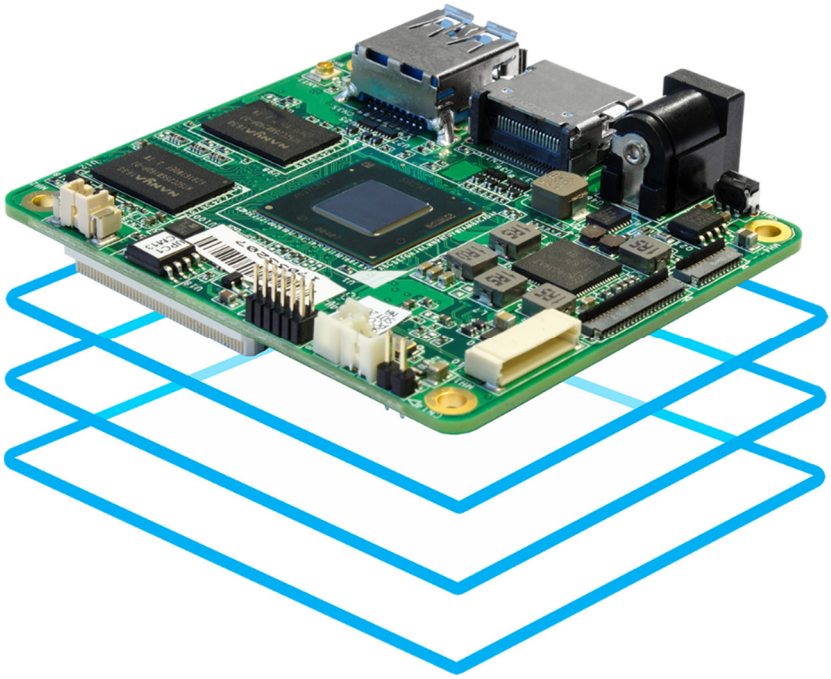
UP CORE Carrier Board Design Guide



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Established in 1992, AAEON is one of the leading designers and manufacturers of advanced industrial and embedded computing platforms today.

Committed to innovative engineering, AAEON provides integrated solutions, hardware and services for premier OEM/ODMs and system integrators worldwide. Reliable and high quality computing platforms include industrial motherboards and systems, industrial displays, rugged tablets, PC/104, PICMG and COM modules, embedded SBCs, embedded controllers, network appliances and related accessories. AAEON also offers customized end-to-end services from initial product conceptualization and product development on through to volume manufacturing and after-sales service programs.

With a continuous pursuit of innovation and excellence, AAEON became a member of the ASUS group in 2011, further strengthening its leadership fueled by advanced technology from ASUS and leveraging resources within the group. AAEON is posed to offer more diversified embedded products and solutions at higher quality standards to meet world-class design and manufacturing demands in the years to come.

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Reliability: Delivering trustworthy products on a timely manner to our customers

Integrity: We value business integrity and ethics, making AAEON your choice business partner

Innovation: Working abreast with industry leaders to maintain technology leadership, AAEON is able to help customers turn cutting-edge concepts into reality

Revision History

Version	Release Date	Remark
V0.1	2017/11/15	First release

1.0 UP CORE Carrier board Pinout

Pin	EXPANSION CONNECTOR	Description	Plat. Power	Pwrgood Assert State
A1	5V	Power supply MB to carrier board or carrier board to MB	Voltage tolerance DC±2% , per pin 0.5A	
A2	5V	Power supply MB to carrier board or carrier board to MB	Voltage tolerance DC±2% , per pin 0.5A	
A3	5V	Power supply MB to carrier board or carrier board to MB	Voltage tolerance DC±2% , per pin 0.5A	
A4	5V	Power supply MB to carrier board or carrier board to MB	Voltage tolerance DC±2% , per pin 0.5A	
A5	5V	Power supply MB to carrier board or carrier board to MB	Voltage tolerance DC±2% , per pin 0.5A	
A6	5V	Power supply MB to carrier board or carrier board to MB	Voltage tolerance DC±2% , per pin 0.5A	
A7	5V	Power supply MB to carrier board or carrier board to MB	Voltage tolerance DC±2% , per pin 0.5A	
A8	5V	Power supply MB to carrier board or carrier board to MB	Voltage tolerance DC±2% , per pin 0.5A	
A9	GND	GND		
A10	GND	GND		
A11	PMU_RSTBTN_N	**System Reset:** This signal forces an internal reset after being debounced.	V1P8	Input 20k PULL UP
A12	UART1_RTS	High-speed request to send	V1P8	Buffer drives VOH , 20k PULL UP
A13	PMU_PWRBTN_N	**Power Button:** The signal will cause SMI_N or SCI to indicate a system request to go to a	V1P8	Input 20k PULL UP

		sleep state. If the system is already in a sleep state, this signal will cause a wake event. If the signal is pressed for more than 4 seconds, this will cause an unconditional transition (power button override) to the S5 state. Override will occur even if the system is in the S4 states. This signal has an internal pull-up resistor and has an internal 16 ms de-bounce on the input.		
A14	UART1_CTS	High-speed clear to send	V1P8	Input 20k PULL UP
A15	PMU_SLP_S0IX_N	**S0ix Sleep Control:** This signal is for power plane control. It can be used to control system power when it is in a S0ix state.	V1P8	20k PULL UP
A16	GPIO16/UART1_TX	High-speed transmit data	V1P8	Buffer drives VOH , 20k PULL UP
A17	PCIE_CLKREQ0	**PCI Express* Clock Request** Used for devices that need to request one of the output clocks. Each clock request maps to the matching PCIe Root Port (e.g. PCIE_CLKREQ#[0] maps to PCIE Root Port [0] and so on) **NOTE:** These signals are muxed and may be used by other functions.	V1P8	Input 20k PULL UP

A18	GPIO17/UART1_RX	High-speed receive data input	V1P8	Input 20k PULL UP
A19	PMC_SUSCLK0	**Suspend Clock:** This 32 kHz clock is an output of the RTC generator circuit for use by other chips for refresh clock. *This signal is muxed and may be used by other functions.*	V1P8	Buffer drives VOL , (20k PULL DOWN)
A20	GND	GND		
A21	GND	GND		
A22	DDI2_DDC_CLK	Display I2C interface	V1P8	The SoC places this output in a high-impedance state. For inputs, external drivers are not expected.
A23	GPIO7/HAT_SPI2_MOSI	**SPI Master OUT Slave IN:** Data output pin for the SoC. Operates as a second data input pin for the SoC when in Single Input, Dual Output Fast Read mode.	V1P8	Buffer drives VOL , 20k PULL UP
A24	DDI2_DDC_DAT	Display I2C interface	V1P8	The SoC places this output in a high-impedance state. For inputs, external drivers are not expected.
A25	GPIO8/SPI_MISO	**SPI Master IN Slave OUT:** Data input pin for the SoC.	V1P8	Input 20k PULL UP
A26	HDMI_CEC_D	For CPLD control	V1P8	RESERVED

A27	GPIO9/SPI_CLK	**SPI Clock:** When the bus is idle, the owner will drive the clock signal low.	V1P8	Buffer drives VOL , 20k PULL UP
A28	HDMI_CEC_R	For CPLD control	V1P8	RESERVED
A29	GPIO22/SPI_CS0N	**SPI Chip Select 0:** Used as the SPI Chip select 0.	V1P8	Buffer drives VOH , 20k PULL UP
A30	DDI2_TYPE_C_HPD	Hot Plug Detect	V1P8	Input (20k PULL DOWN)
A31	GPIO23/SPI_CS1N	**SPI Chip Select 1:** Used as the SPI Chip select 1.	V1P8	Buffer drives VOH , 20k PULL UP
A32	ISH_GPIO0	ISH_GPIO0	V1P8	Weak internal 20k PULL DOWN
A33	GND	GND		
A34	CPLD CLEAR/ISH_GPIO1	CPLD CLEAR/ISH_GPIO1	V1P8	Weak internal 20k PULL DOWN
A35	RESERVE	N/A		
A36	ISH_GPIO2	ISH_GPIO2	V1P8	Weak internal 20k PULL DOWN
A37	RESERVE	N/A		
A38	ISH_GPIO3	ISH_GPIO3	V1P8	Weak internal 20k PULL DOWN
A39	RESERVE	N/A		

A40	ISH_GPIO4	ISH_GPIO4	V1P8	Weak internal 20k PULL DOWN
A41	RESERVE	N/A		
A42	CPLD DIN/ISH_GPIO7	CPLD DIN/ISH_GPIO7	V1P8	Weak internal 20k PULL DOWN
A43	GND	GND		
A44	ISH_GPIO9	ISH_GPIO9	V1P8	Weak internal 20k PULL DOWN
A45	GPIO18/I2S2_CLK	Clock signal for I2S	V1P8	Input 20k PULL DOWN
A46	GPIO25/PWM0	Pulse Width Modulation output 0.	V1P8	Buffer drives VOL , 20k PULL DOWN
A47	GPIO14/I2S2_FRM	Frame select signal for I2S	V1P8	Input 20k PULL DOWN
A48	GPIO13/PWM1	Pulse Width Modulation output 1.	V1P8	Buffer drives VOL , 20k PULL UP
A49	GPIO27/I2S2_DATAIN	RX data for I2S	V1P8	Input 20k PULL DOWN
A50	GND	GND		
A51	GPIO28/I2S2_DATAOUT	TX data for I2S	V1P8	Buffer drives VOL , 20k PULL UP
A52	USB_HSIC_1_DATA	**HSIC Data**	V1P2	**Weak** Buffer drives VOL

A53	GND	GND		
A54	USB_HSIC_1_STROBE	**HSIC Strobe**	V1P2	**Weak** Buffer drives VOH
A55	PCIE_TX0_DP	PCI Express Transmit Differential-Pair	V1P05	
A56	GND	GND		
A57	PCIE_TX0_DN	PCI Express Transmit Differential-Pair	V1P05	
A58	USB_HSIC_2_DATA	**HSIC Data**	V1P2	**Weak** Buffer drives VOL
A59	GND	GND		
A60	USB_HSIC_2_STROBE	**HSIC Strobe**	V1P2	**Weak** Buffer drives VOH
A61	PCIE_RX0_DP	PCI Express Receive Differential-Pair	V1P05	
A62	GND	GND		
A63	PCIE_RX0_DN	PCI Express Receive Differential-Pair	V1P05	
A64	USB2_P6_DP	Universal Serial Bus Port Differential	V1P8	"P" 1.1V
A65	GND	GND		
A66	USB2_P6_DN	Universal Serial Bus Port Differential	V1P8	"P" 1.1V
A67	PCIE_REFCLK0_DP	PCI Express Reference clock Differential-Pair	V1P05	
A68	GND	GND		
A69	PCIE_REFCLK0_DN	PCI Express Reference clock Differential-Pair	V1P05	x

A70	USB_OTG_R_ID	USB OTG ID pin	V1P8	Input, weak pull up
A71	GND	GND		
A72	GND	GND		
A73	I2C0_SOC_SDA	I2C0 data	V1P8	The SoC places this output in a high-impedance state. (1k PU, OD)
A74	SD3_CD	SD Card detect	V1P8	Input (20k PU)
A75	I2C0_SOC_SCL	I2C0 clock	V1P8	The SoC places this output in a high-impedance state. (1k PU, OD)
A76	SD3_CMD	SD Card command	V1P8/ V3P3	The SoC places this output in a high-impedance state. 20k PULL UP
A77	GND	GND		
A78	SD3_1P8_EN	SD Card 1.8V Enable	V1P8	Buffer drives VOL , 20k PULL DOWN
A79	I2C1_SOC_SDA	I2C1 data	V1P8	Input 20k PULL UP
A80	SD3_PWREN	SD Card power enable	V1P8	Buffer drives VOH ,

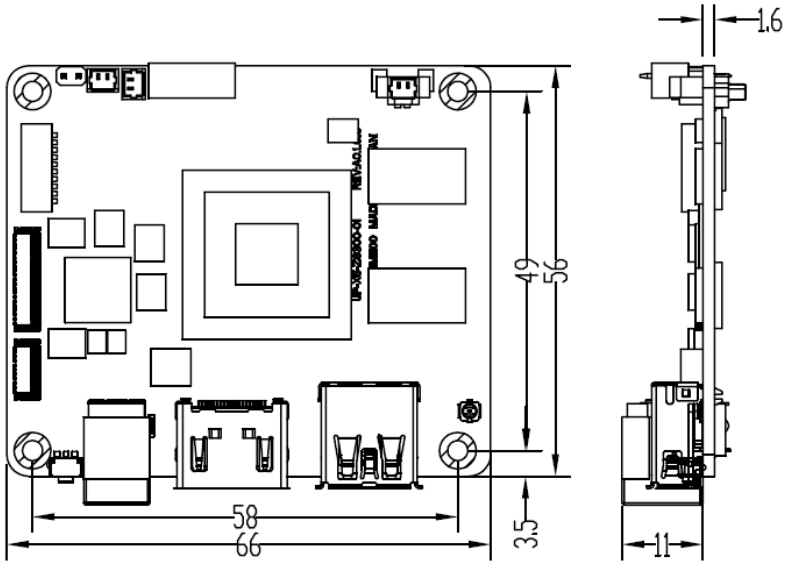
				20k PULL DOWN
A81	I2C1_SOC_SCL	I2C1 clock	V1P8	Input 20k PULL UP
A82	SD3_WP	SD Card write protect	V1P8	Buffer drives VOL , 20k PULL DOWN
A83	GND	GND		
A84	SD3_CLK	SD Card clock	V1P8/ V3P3	Buffer drives VOL , 20k PULL DOWN
A85	CPLD DOUT/ISH_I2C1_ DATA	CPLD DOUT/ISH_I2C1_DATA	V1P8	Input 20k PULL UP
A86	SD3_SD0	SD Card data bit 0	V1P8	The SoC places this output in a high-impedance state. 20k PULL UP
A87	ISH_I2C1_CLK	ISH_I2C1_CLK	V1P8	Input (20k PU)
A88	SD3_SD1	SD Card data bit 1	V1P8	The SoC places this output in a high-impedance state. 20k PULL UP
A89	GND	GND		
A90	SD3_SD2	SD Card data bit 2	V1P8	The SoC places this output in a high-impedance state. 20k PULL UP

A91	RESERVE	N/A		
A92	SD3_SD3	SD Card data bit 3	V1P8	The SoC places this output in a high-impedance state. 20k PULL UP
A93	RESERVE	N/A		
A94	GND	GND		
A95	RESERVE	N/A		
A96	CPLD_OE/GPIO_SW78	CPLD_OE/GPIO_SW78	V1P8	Weak internal 20k PULL DOWN
A97	RESERVE	N/A		
A98	CPLD_RST/GPIO_SUS8	CPLD_RST/GPIO_SUS8	V1P8	Weak internal 20k PULL DOWN
A99	RESERVE	N/A		
A100	CPLD_STROBE/GPIO_SUS9	CPLD_STROBE/GPIO_SUS9	V1P8	Weak internal 20k PULL DOWN

2.0 UP CORE Mechanical Specification

2.1 UP CORE Module Form Factors

TOP SIDE:



BOTTOM SIDE:

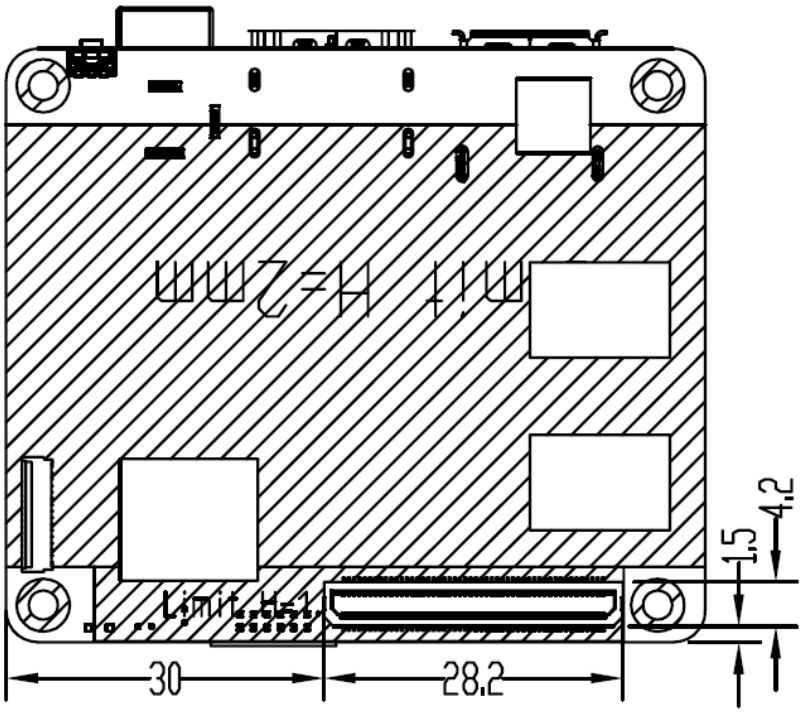


Figure 2-1 Module Form Factors

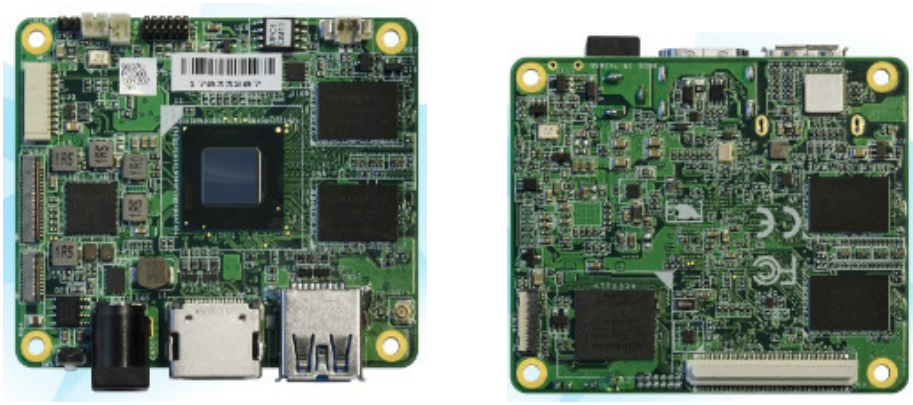


Figure 2-1 AAEON UP CORE Module

2.2 UP CORE Carrier Board Connectors

UP CORE M/B module utilizes one 100-pin high density connectors to interface the UP CORE module and carrier board. To design Carrier Board Connector:

Connector Socket type : PANASONIC / AXK5S00347YG

Mated Height : 9 mm

AXK(5(S)/6(S))

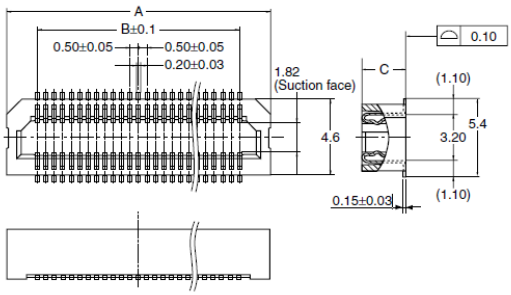
P5KS: Mated height 4.0mm, 4.5mm, 5.0mm, 5.5mm, 6.0mm, 6.5mm, 7.0mm, 8.0mm, 9.0mm type

• Socket

CAD Data

Dimension table (mm)

No. of pins	A	B
20	8.20	4.50
24	9.20	5.50
30	10.70	7.00
34	11.70	8.00
36	12.20	8.50
40	13.20	9.50
50	15.70	12.00
60	18.20	14.50
70	20.70	17.00
80	23.20	19.50
100	28.20	24.50



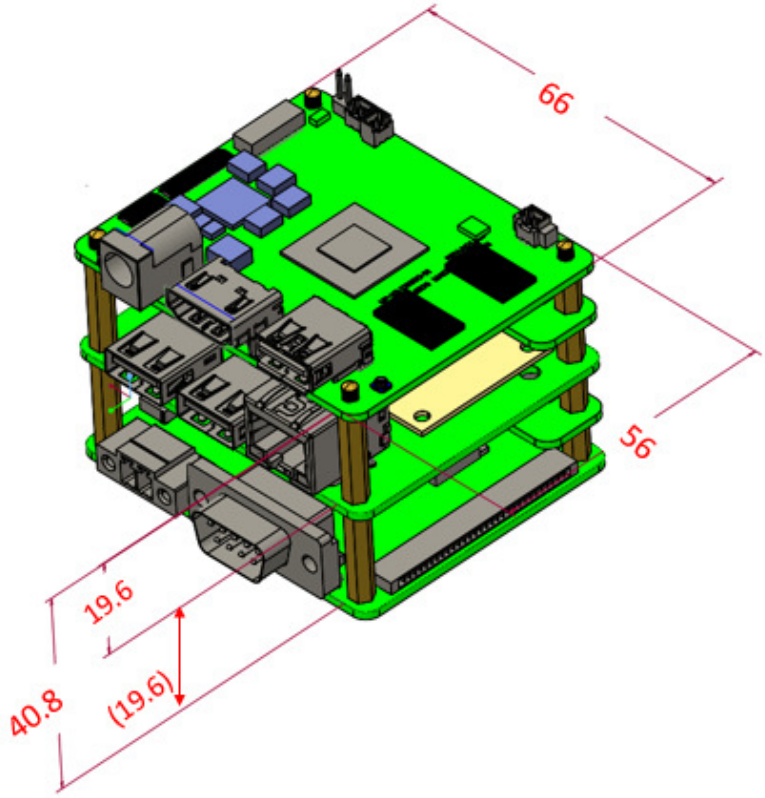
General tolerance: ±0.2

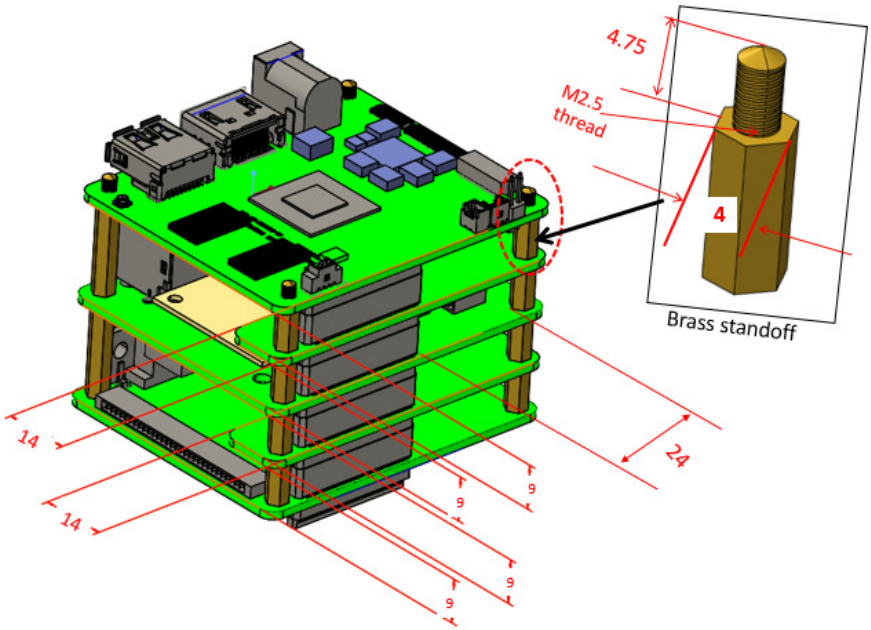
Mated height	C
4.0 mm, 5.0 mm, 6.0 mm	3.05
4.5 mm, 5.5 mm, 6.5 mm	3.55
7.0 mm, 8.0 mm, 9.0 mm	6.05

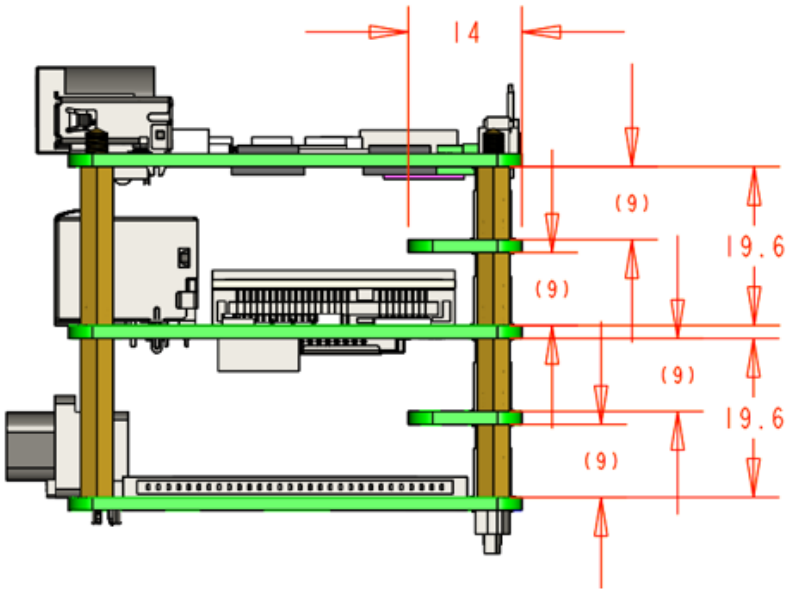
Figure 2-2-1 Carrier Board Connector

2.3 PCB dimension reference

2.3.1 UP CORE system reference

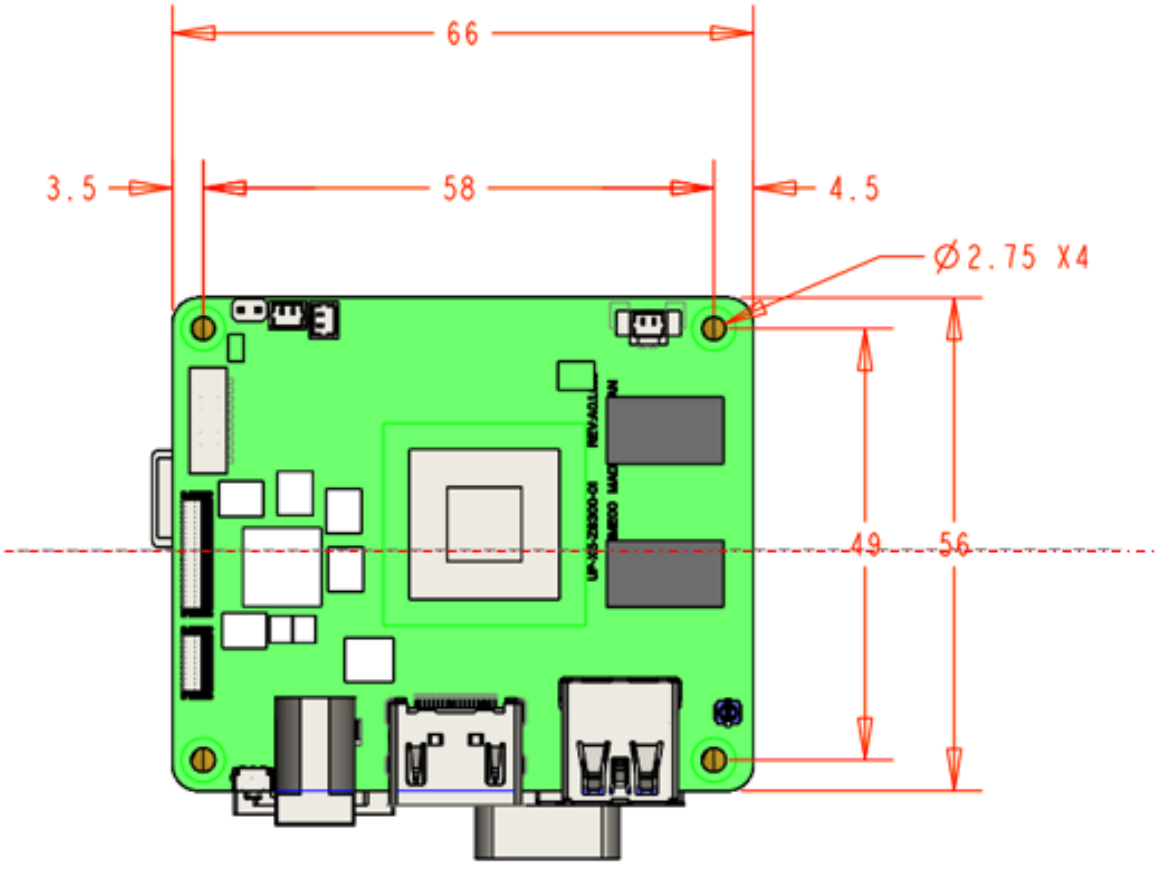




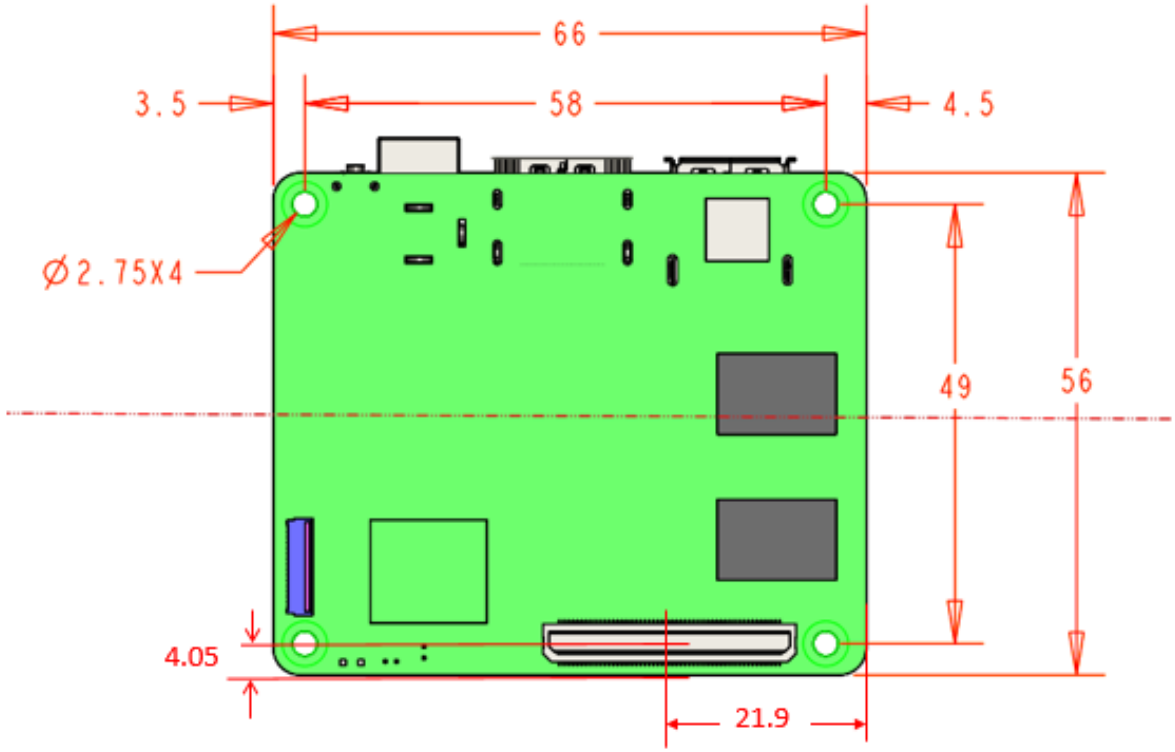


2.3.2 UP CORE MB

TOP SIDE:

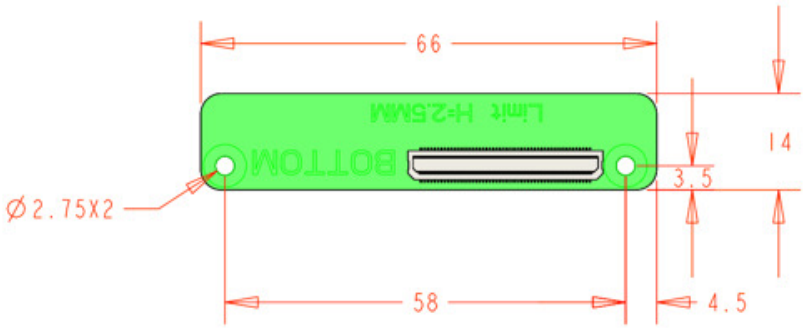


BOTTOM SIDE:

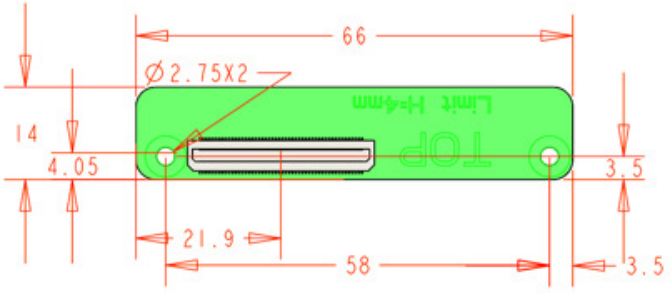


2.3.3 Spacer Carrier board

TOP SIDE

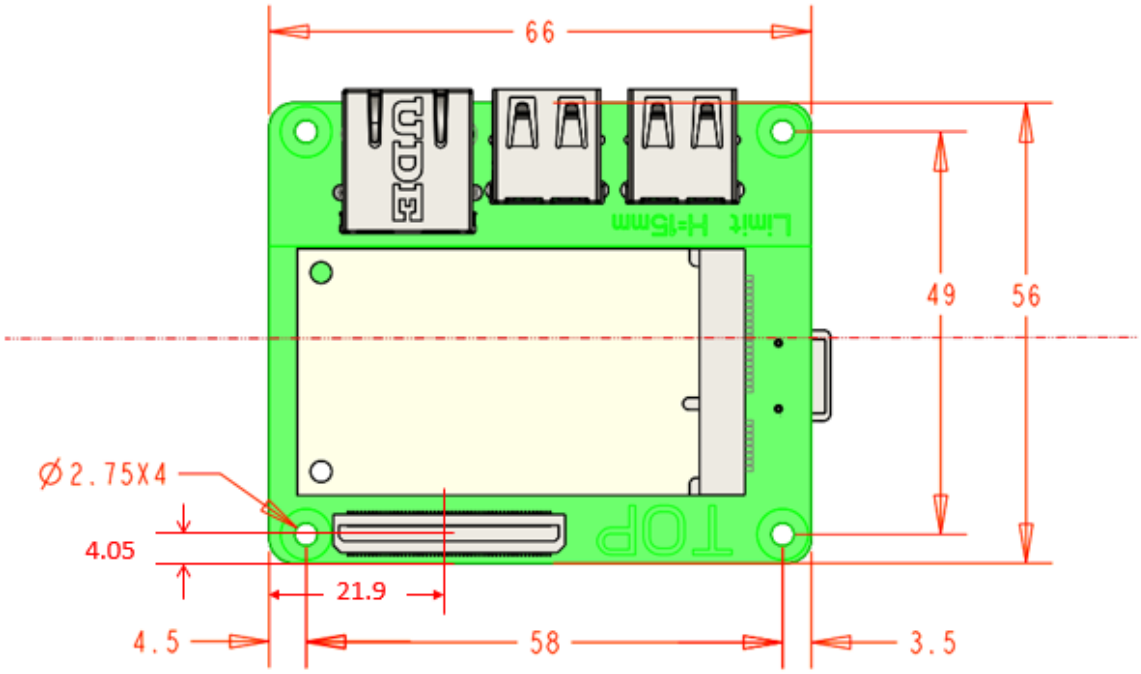


BACK SIDE

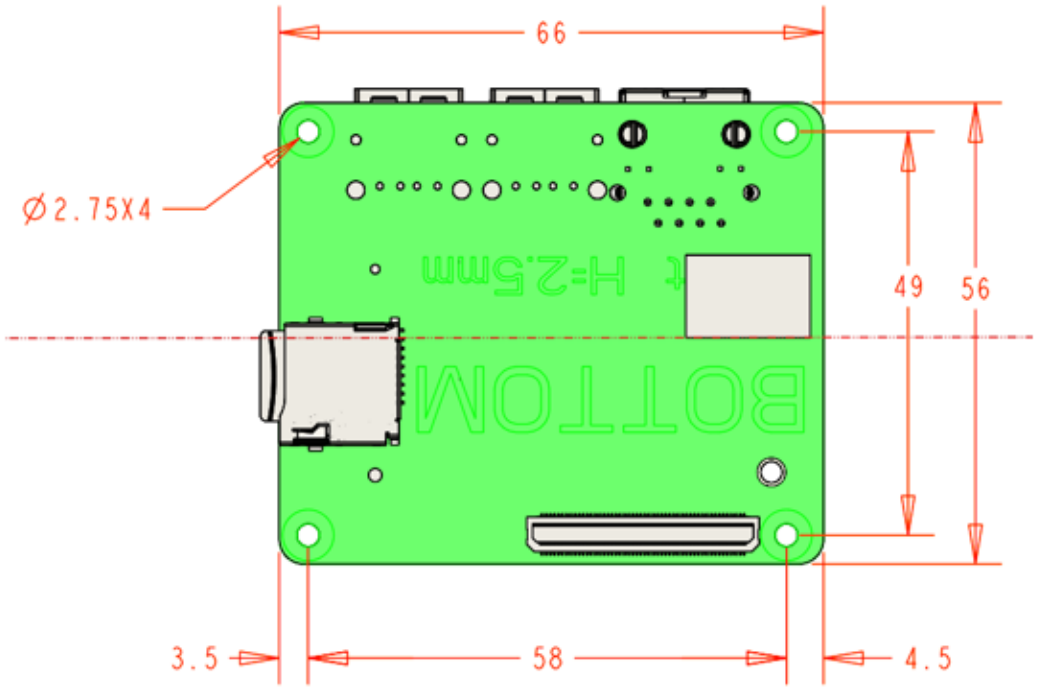


2.3.4 Carrier board (user customize)

TOP SIDE:



BOTTOM SIDE



3.0 PCB STACK

3.1 PCB Stack Example

NO.	LAYER DESCRIPTION	stack up design	After pressing the thickness of each layer and copper thickness(mil)	ORIGINAL (mil)		REFERENCEL AYER	IMPEDANCE TYPE	IMPEDANCE SPEC(ohms±%)
				TRACE	SPACE			
Solder Mask			0.5					
Layer 1	TOP	0.5oz+plating	1.8	4		L2	single end	50±10%
				4	5	L2	differential pair	85±10%
				3.5	12	L2	differential pair	100±15%
Prepreg		1080 HR	2.8					
Layer 2	GND1	1 oz	1.3					
Core		4 mil	4					
Layer 3	IN1	1 oz	1.3	5.2		L2，L5	single end	50±10%
				4	4	L2，L5	differential pair	85±10%
				3.5	6.5	L2，L5	differential pair	100±15%
Prepreg		core 24mil + 7628*2	38					
Layer 4	VCC	1 oz	1.3					
Core		4 mil	4					
Layer 5	GND2	1 oz	1.3					
Prepreg		1080 HR	2.8					
Layer 6	BOTTOM	0.5oz+plating	1.8	4		L5	single end	50±10%
				4	5	L2	differential pair	85±10%
				3.5	12	L2	differential pair	100±15%
Solder Mask			0.5					
PCB THICKNESS			**64 mil**					

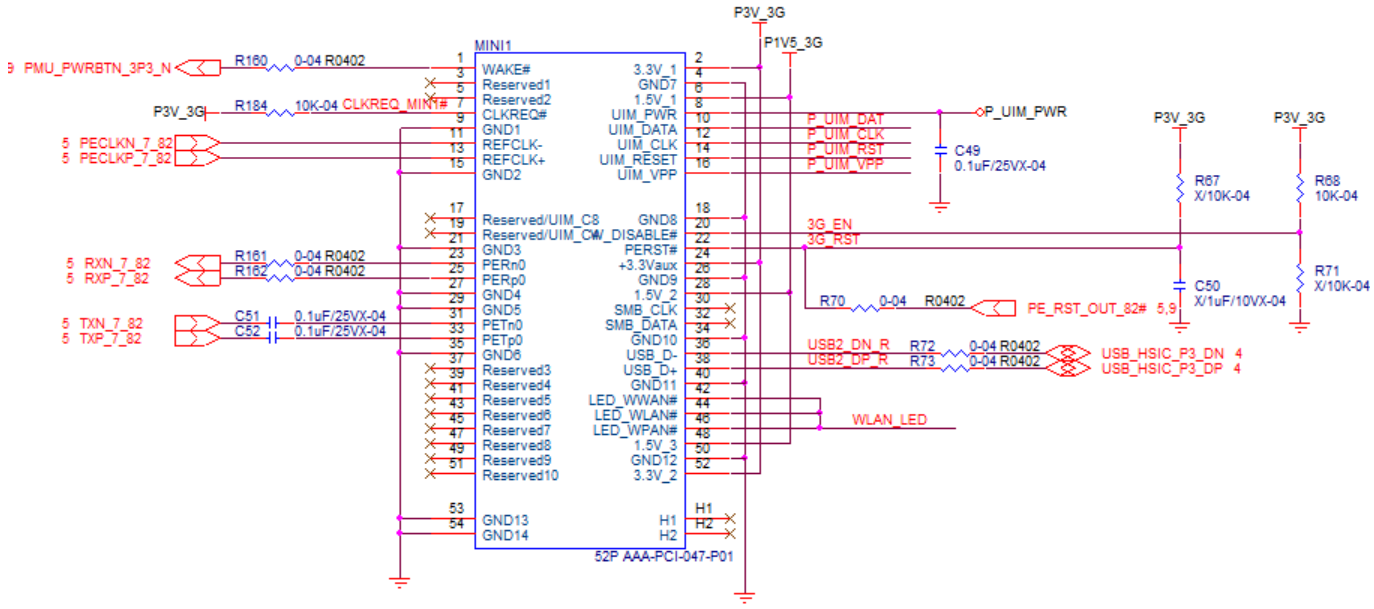
Design should follow above impedance value

3.2 Main routing general layout requirement

I/O Interfaces	Stackup	Electrical Target				Layout Geometries (mils)			
		Zo (Ohms)	Zdiff (Ohms)	Kb (%)	Kb (%) Isolation to Next signal group	Trace Width	Differential intra-pair spacing	Spacing (Within Signal Group)	Isolation (to Other Signal Groups)
eDP	MS	50	85	3.2	1.57	4	5	8	12
eDP	DSL	50	85	3.2	1.57	4	4.5	8	12
DP	DSL	50	85	3.2	1.57	4	4.5	8	12
MIPI-DSI	DSL	50	85	3.2	1.57	4	4.5	8	12
MIPI-CSI	DSL	50	85	3.2	1.57	4	4.5	8	12
USB3	MS	50	85	3.2	1.57	4	5	8	12
USB3	DSL	50	85	3.2	1.57	4	4.5	8	12
USB2	MS	50	85	3.2	1.57	4	5	8	12
USB2	DSL	50	85	3.2	1.57	4	4.5	8	12
PCIe	DSL	50	85	3.2	1.57	4	4.5	8	12
XTAL IN/OUT	MS/DSL	50	N/A	0.8	0.8	4	N/A	15	15
Platform CLK	MS/DSL	50	N/A	1.57	0.8	4	N/A	12	15
eMMC DATA	DSL	50	N/A	3.2	3.2	4	N/A	8	8
eMMC CLK	DSL	50	N/A	1.57	0.8	4	N/A	12	15
SDIO DATA/CMD	DSL	50	N/A	3.2	3.2	4	N/A	8	8
SDIO CLK	DSL	50	N/A	3.2	1.57	4	N/A	8	12
HSIC DATA	DSL	50	N/A	3.2	4.0	4	N/A	8	7
HSIC STB	DSL	50	N/A	3.2	0.8	4	N/A	8	15
FSTSPI Data	DSL	50	N/A	3.2	3.2	4	N/A	8	8
FSTSPI CLK	DSL	50	N/A	1.57	0.8	4	N/A	12	15
I2C	DSL	50	N/A	6	4.0	4	N/A	5	7
I2S	DSL	50	N/A	6	4.0	4	N/A	5	7
UART	DSL	50	N/A	6	4.0	4	N/A	5	7
SVID	DSL	50	N/A	6	6.0	4	N/A	5	7

4.0 Circuit Reference

4.1 PCIE Mini-Card Reference Schematics

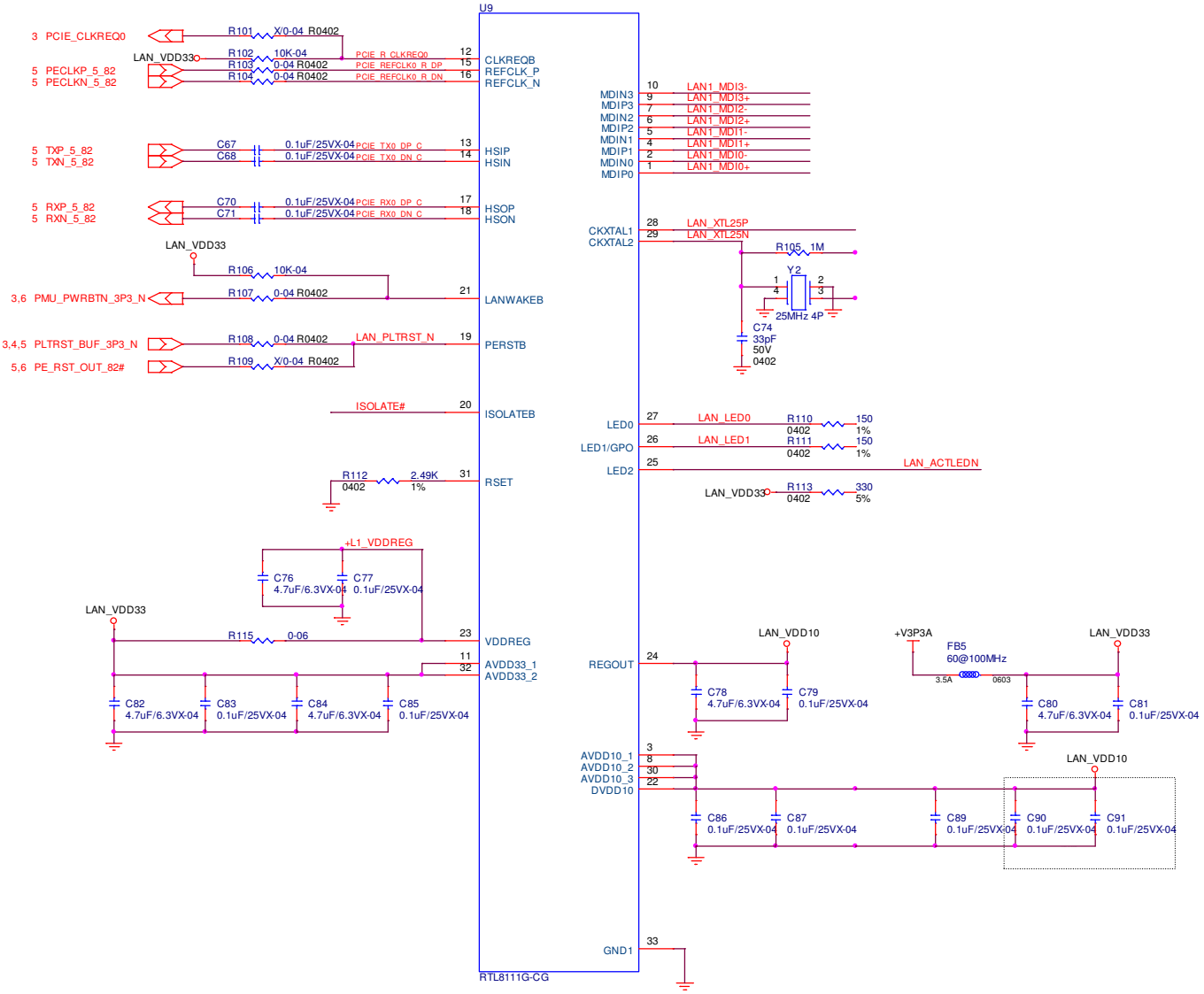


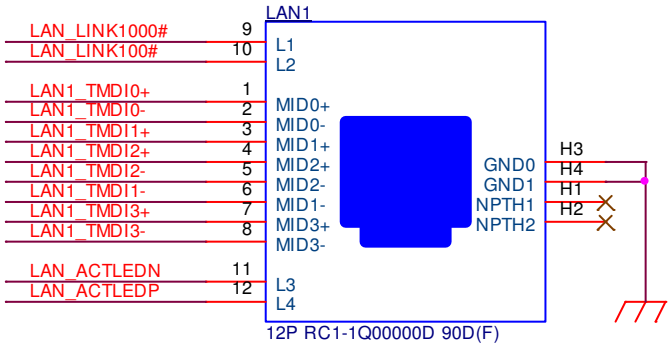
4.2 PCIE LAN Reference Schematics

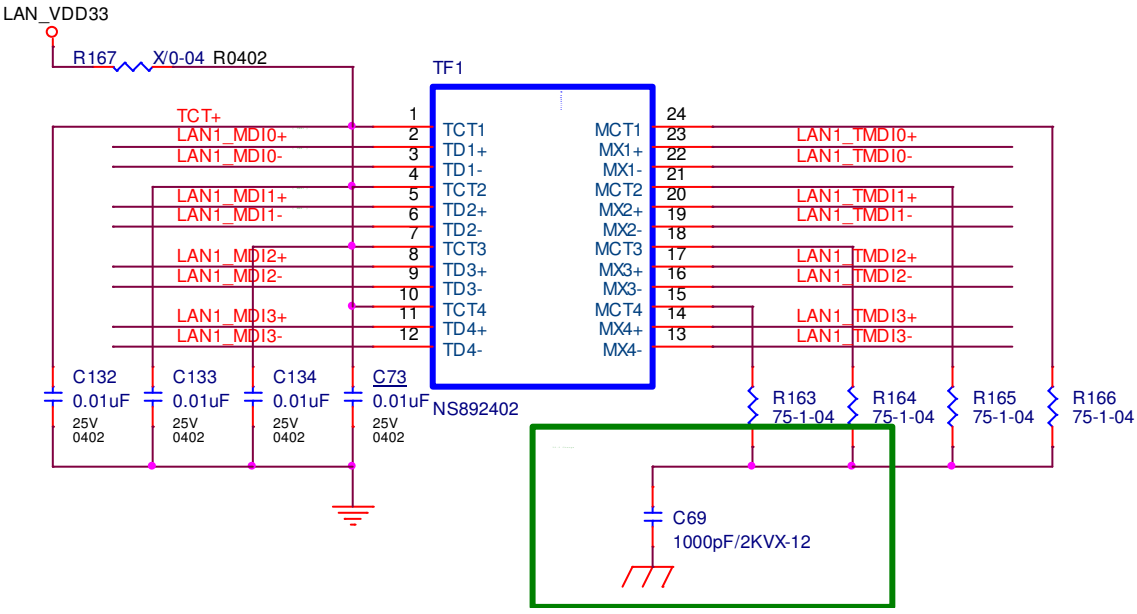
4.2.1 LAN

The 8-wire 10/100/1000BaseT Gigabit Ethernet interface compliant to the IEEE 802.3-2005 specification is the preferred interface for this port, with the carrier Module PHY responsible for implementing auto-negotiation of 10/100BaseTX vs 10/100/1000BaseT operation.

4.2.2 LAN Reference Schematics





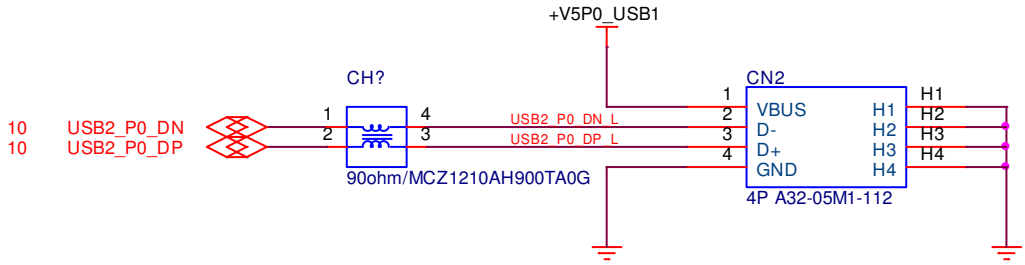


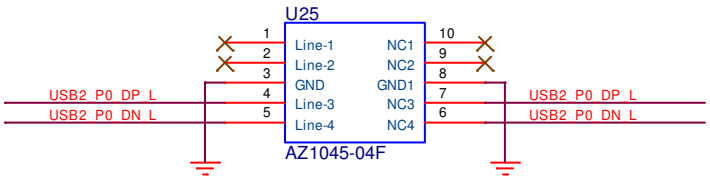
Note: TVS placement must be close to Connector for ESD Solution.

4.3 USB

All USB interfaces shall be USB 2.0 compliant. A Carrier must current limit the USB power source to minimize disruption of the Carrier in the event that a short or over-current condition exists on one of the USB Ports. A Module must fill the USB Ports starting at Port 0.

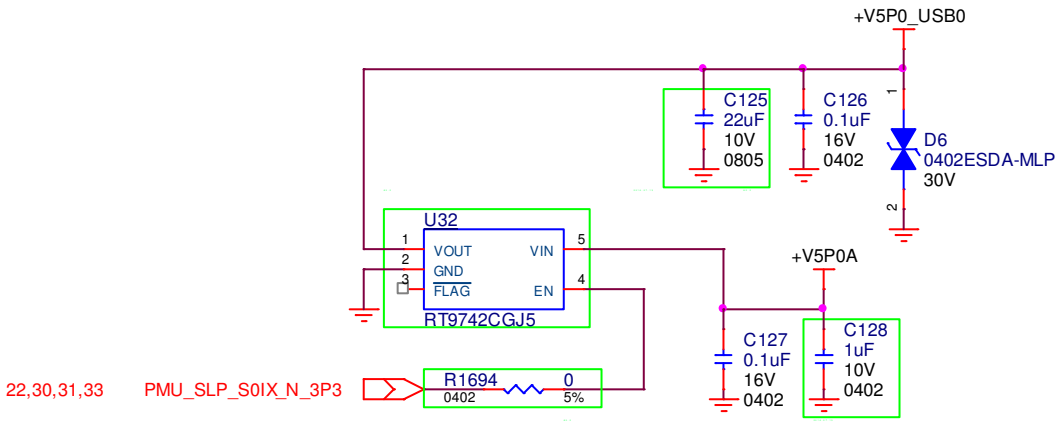
4.3.1 USB Reference Schematics - USB2.





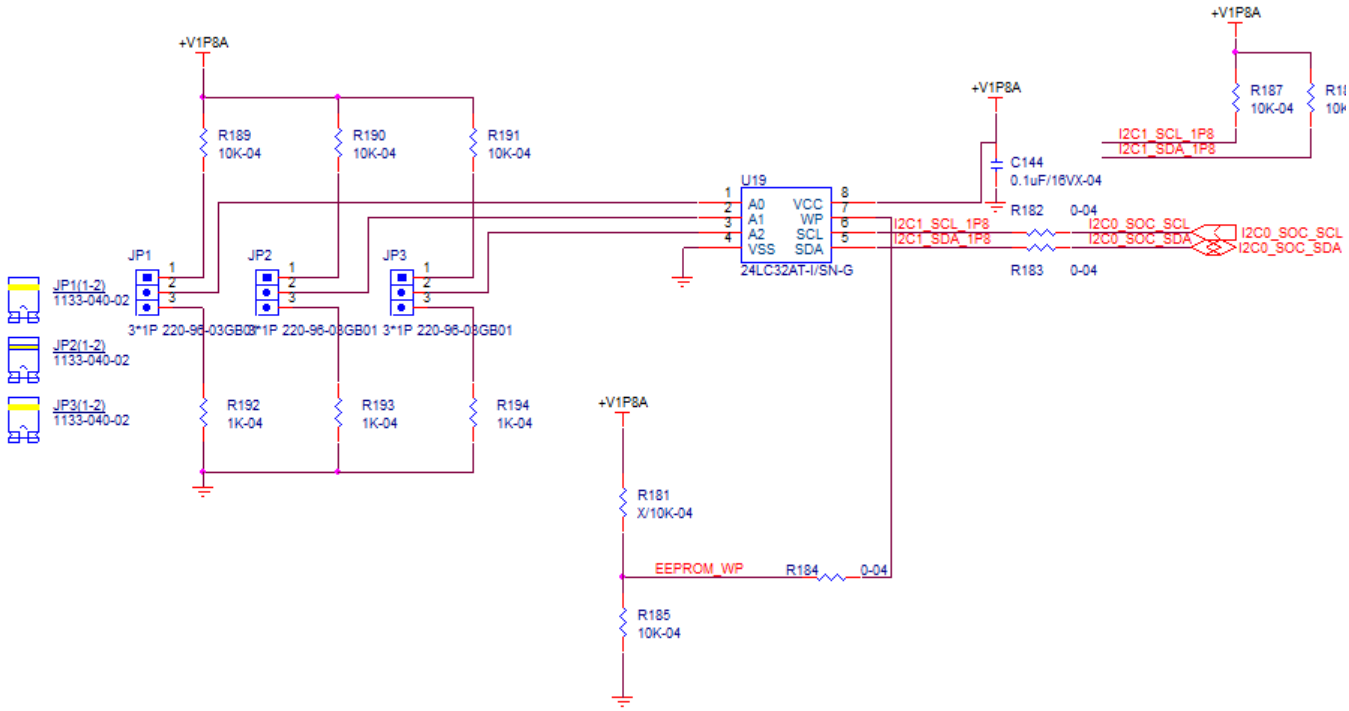
Note: TVS placement must be close to Connector for ESD Solution .

4.3.2 USB Power Over-Current Protection Reference Schematic



4.4 I2C

4.4.1 I2C reference schematic



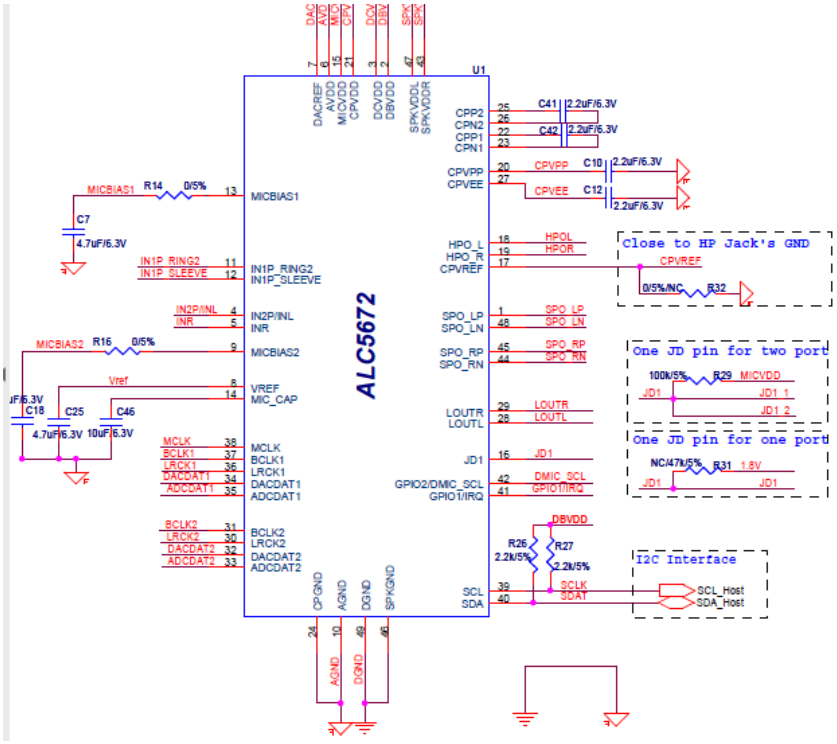
4.5 I2S

SOC LPE Audio subsystem provides HW acceleration for common audio and voice functions such as codec, acoustic echo cancellation, noise cancellation etc. Low Power voice and audio engine provides a mechanism for rendering audio and voice streams and tones from the operating system, applications to an audio or voice codec, and ultimately to the speaker, headphones, or Bluetooth headsets.

I2S port 2 is by default connected to the audio codec.

I2S reference schematic

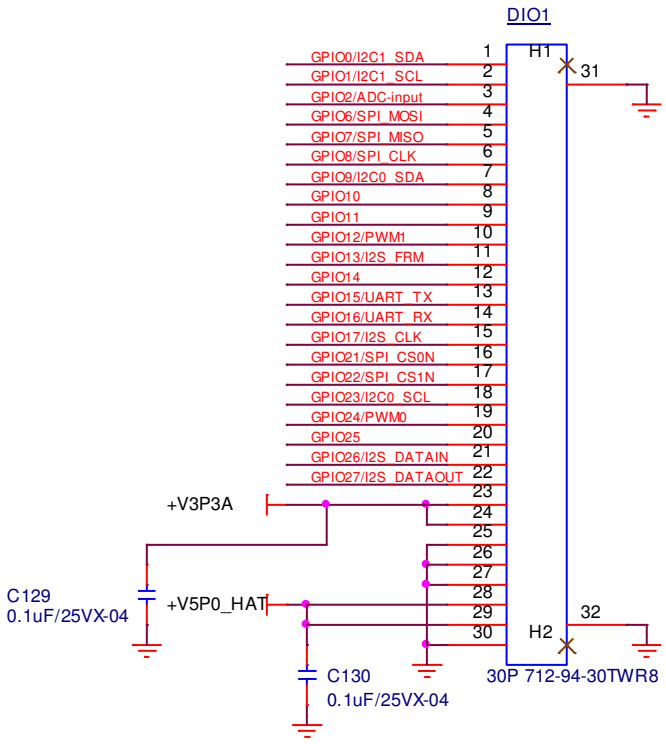
Connect to ALC5672

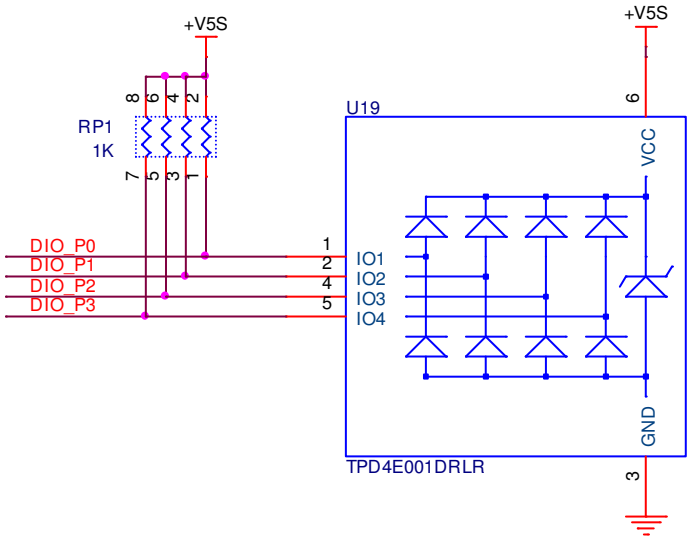


4.6 DIO

General Purpose Input / Output (GPIO)

DIO Reference Schematics

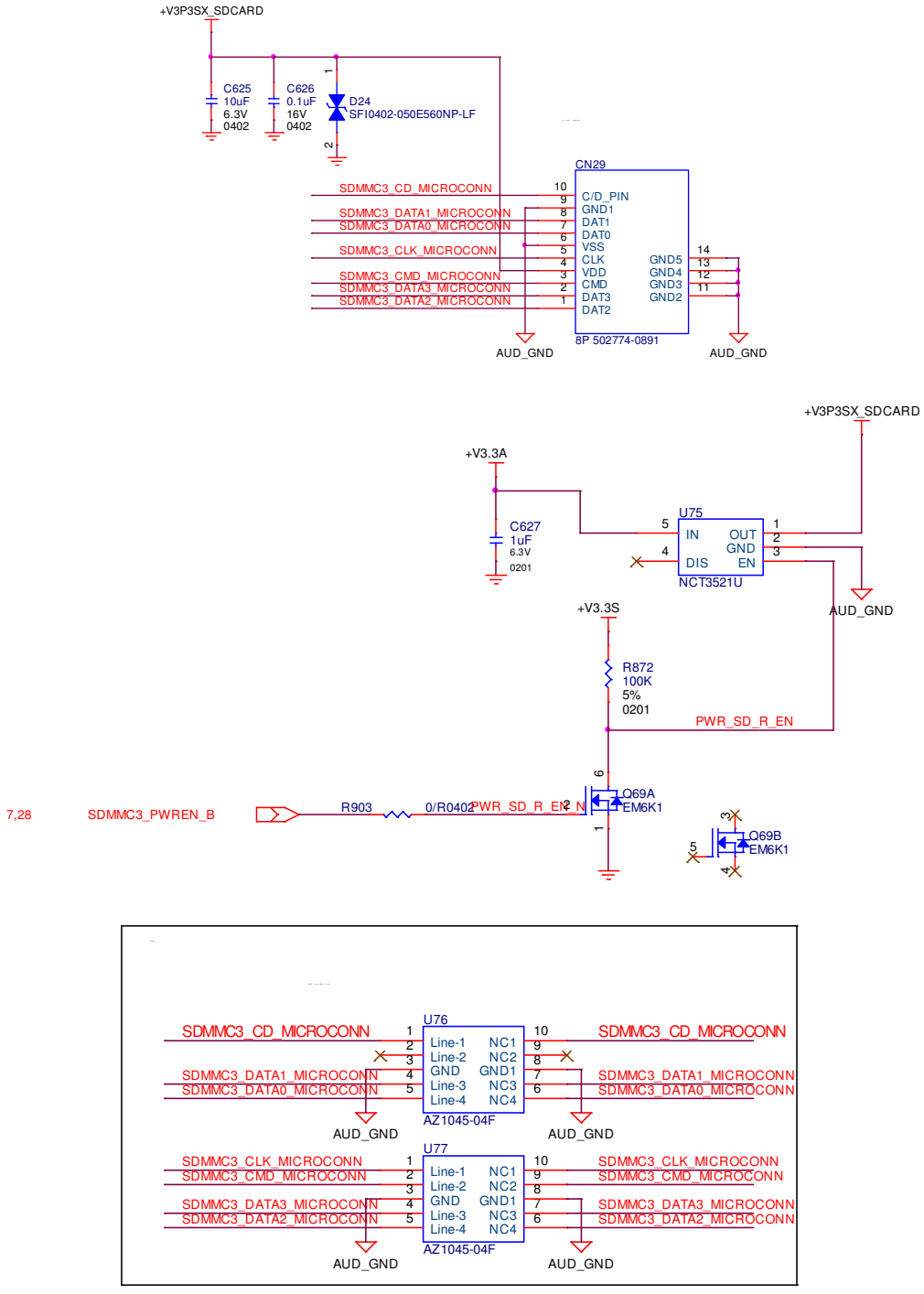




Note: (1) TVS placement must be close to Connector for ESD Solution

4.7 SDIO

SD Card Reference Schematics Note:

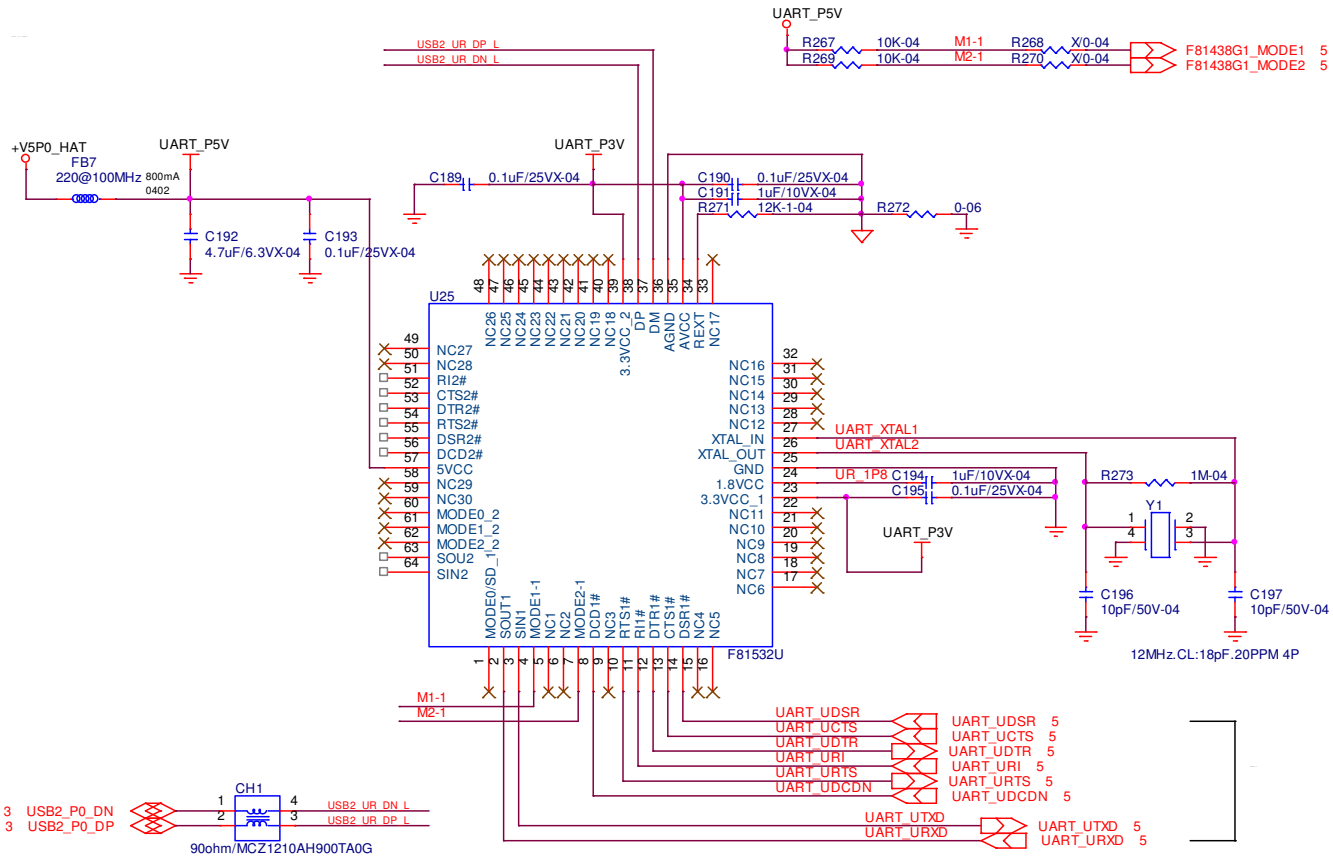


TVS placement must be close to Connector for ESD Solution.

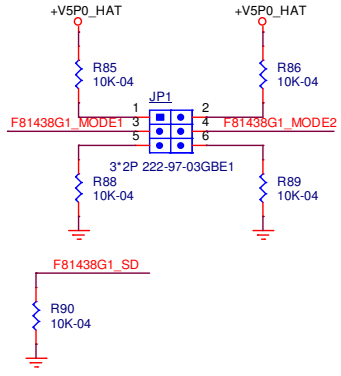
4.8 Serial Interface

Serial Interface Reference Schematics :

4.8.1 USB to UART



4.8.2 UART to RS232/422/485

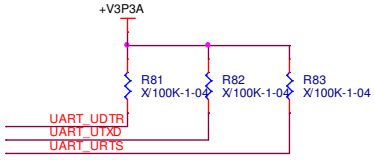


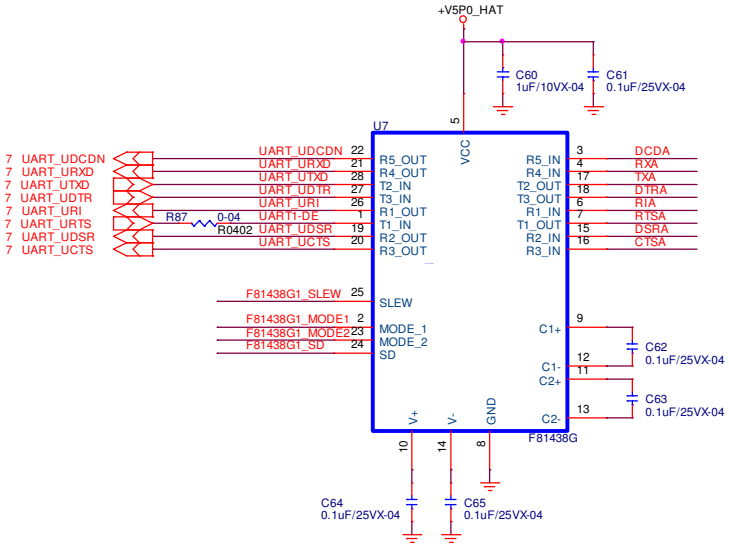
JP1(3-5)1
27S1001-0PS35-01G-R

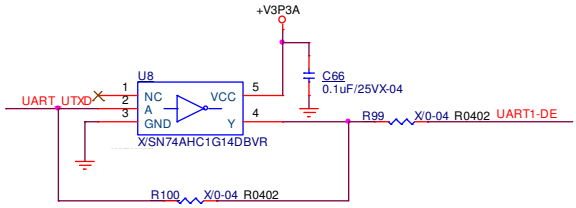
F81438G_MODE1	Selection	
1-3	1	
3-5	0	Default

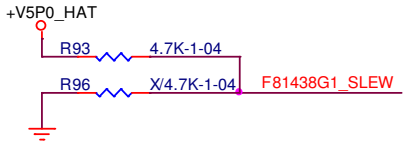
JP1(2-4)1

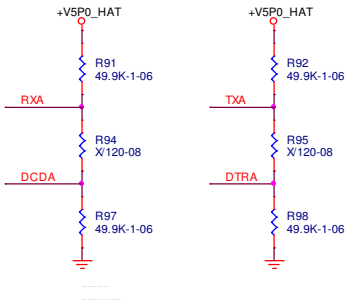
F81438G_MODE2	Selection	
2-4	1	Default
4-6	0	





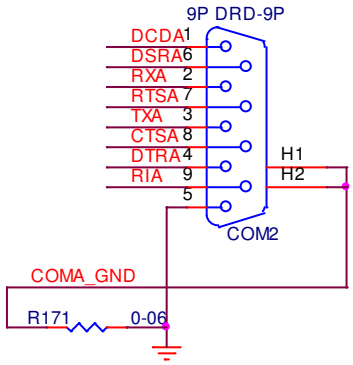






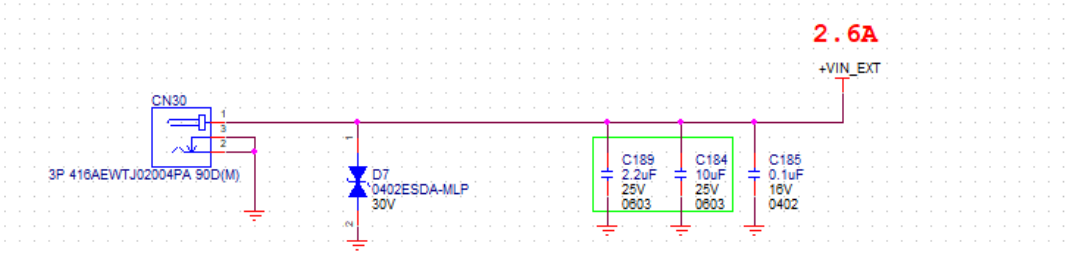
RS-232/485/422 Pin Assignment			
Pin	RS-232	RS-485	RS-422
1	DCD	RS485_D-	RS422_TX-
2	RX	RS485_D+	RS422_TX+
3	TX		RS422_RX+
4	DTR		RS422_RX-

Serlal Port Mode Selection			
SD	Mode_1	Mode_2	Mode
0	0	0	RS-422
0	0	1	RS-232 Default
0	1	1	RS-485
1	X	X	Shutdown Mode

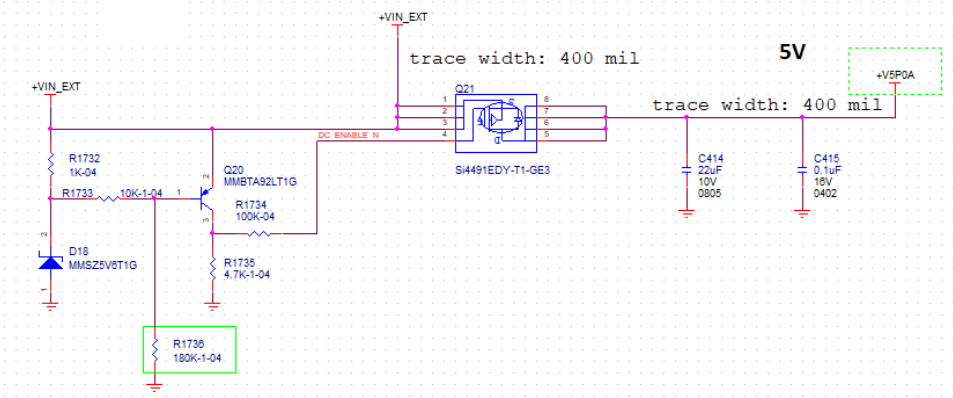


4.9 Power Management Signals

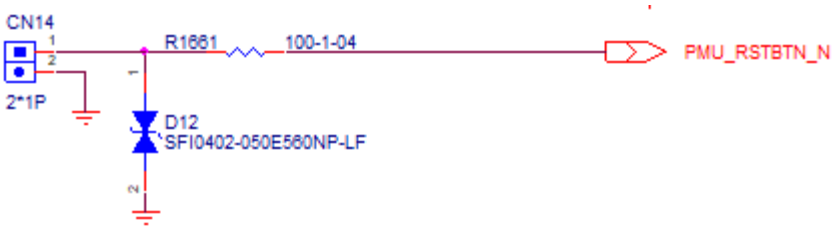
4.9.1 DC IN



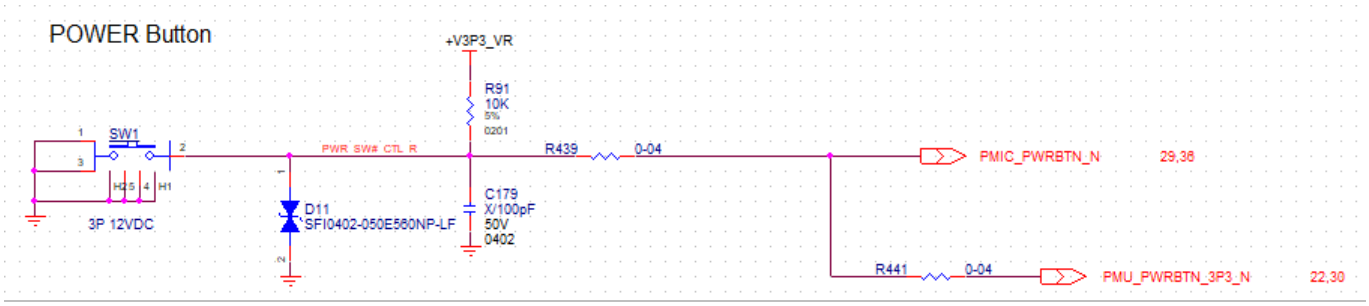
4.9.2 Voltage DC IN Protect circuit



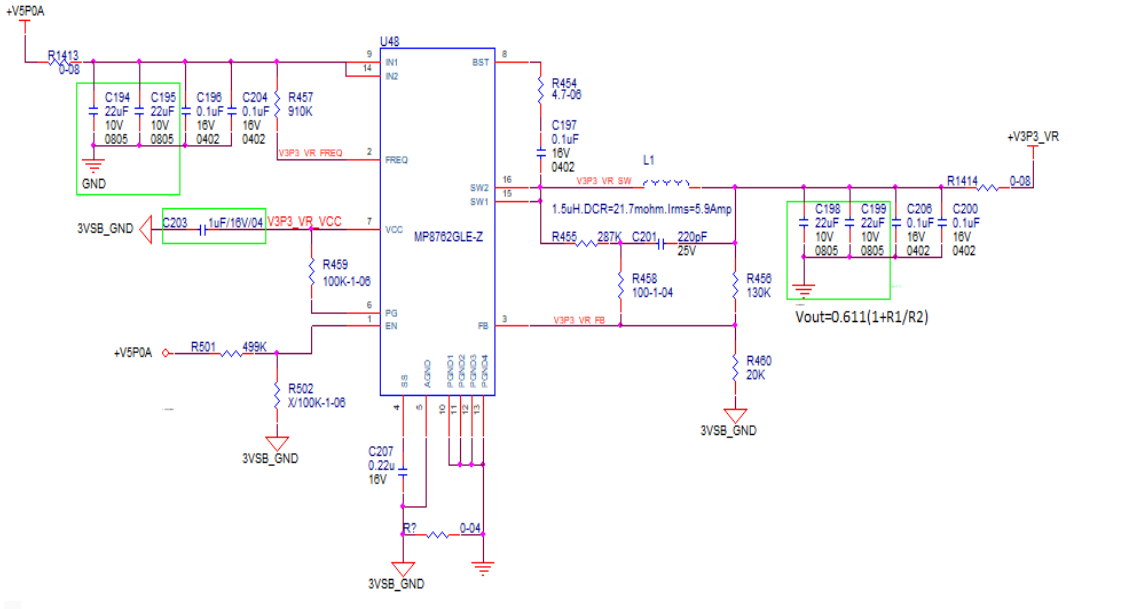
4.9.3 RESET BUTTON



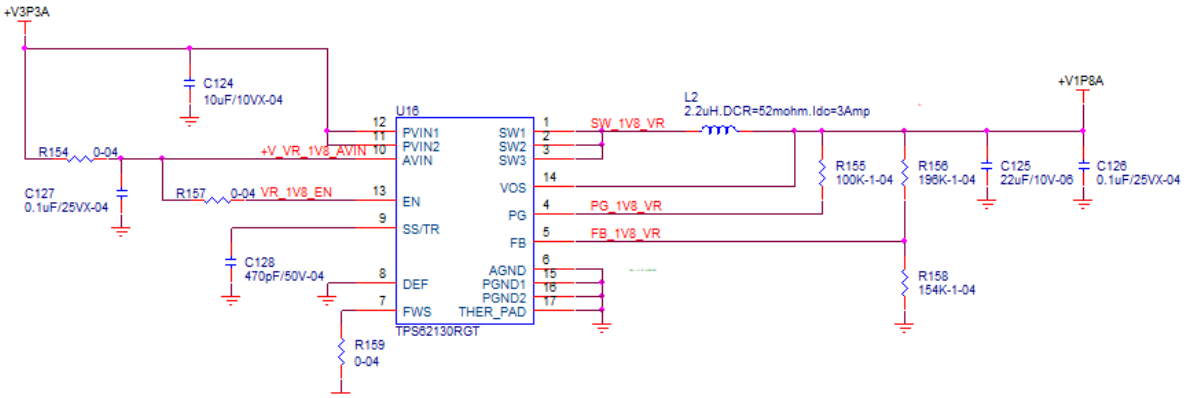
4.9.4 POWER BUTTON



4.9.5 5V to 3.3V CIRCUIT



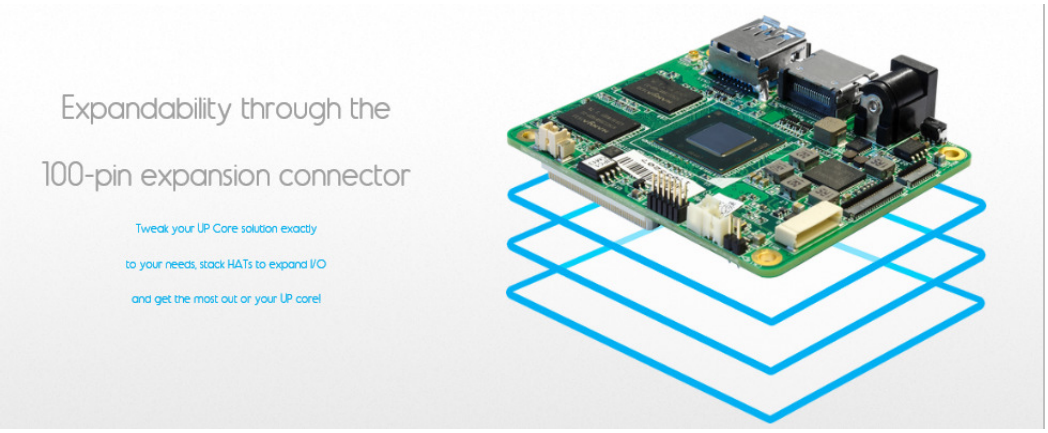
4.9.6 3.3V to 1.8V CIRCUIT



5.0 STACK DESIGN LIMITATION and rule

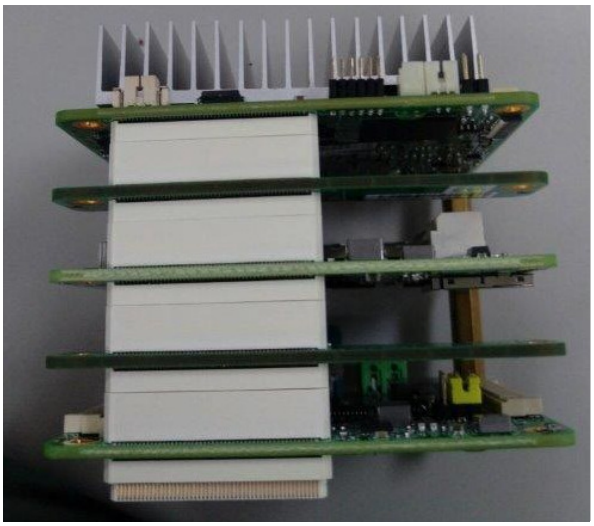
This concept idea is according 100 pin to develop the customize daughter board. The top board is UP CORE MB

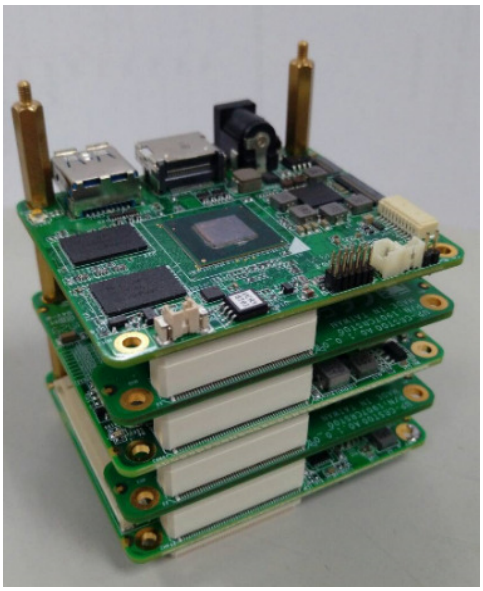
And the second board is the first carrier board which is for high speed signal application only. Then the next carrier board is for power converter and low speed signal application design.



5.1 The Aaeon's current design example:

- Top layer => UP CORE M/B
- Middle layer =>HIGH SPEED Carrier board
- Bottom layer => LOW SPEED Carrier board

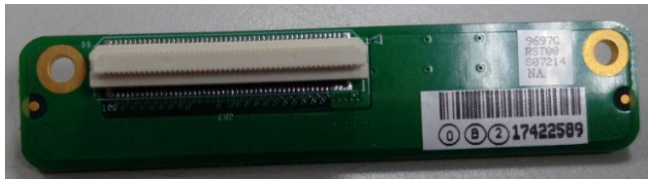




Spacer Carrier board (UP-CRST00) is the bridge between MB & Carrier board and the height is 9mm.

TOP side picture:

Bottom side picture:

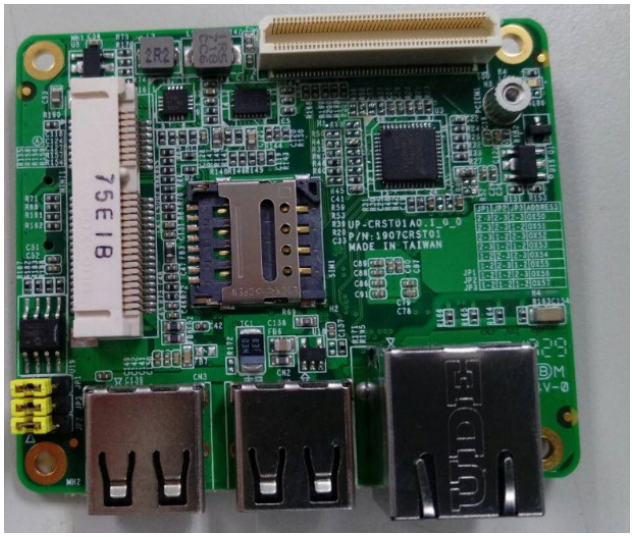


5.2 Signal assignment

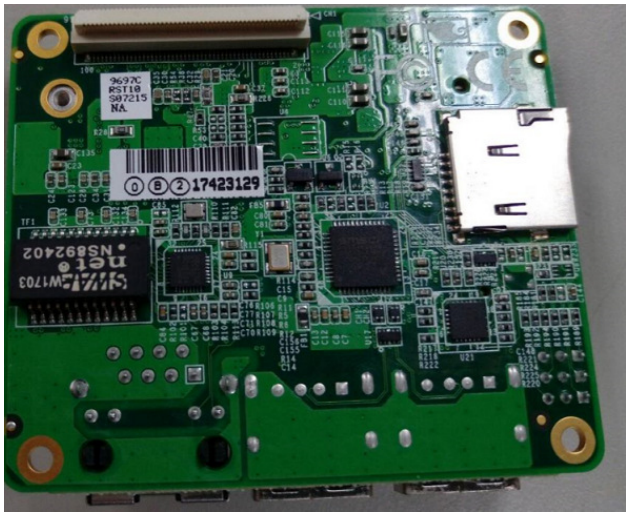
Middle layer (UP-CRST01) =>HIGH SPEED Carrier board include below signal:

- USB
- HSIC
- PCIE
- I2C

TOP side picture



Bottom side picture



Bottom layer (UP-CRST02)=> LOW SPEED Carrier board include below signal :

- Power
- RS232/422/485 (USB to UART)
- I2C
- GPIO
- PWM

TOP side picture

Bottom side picture