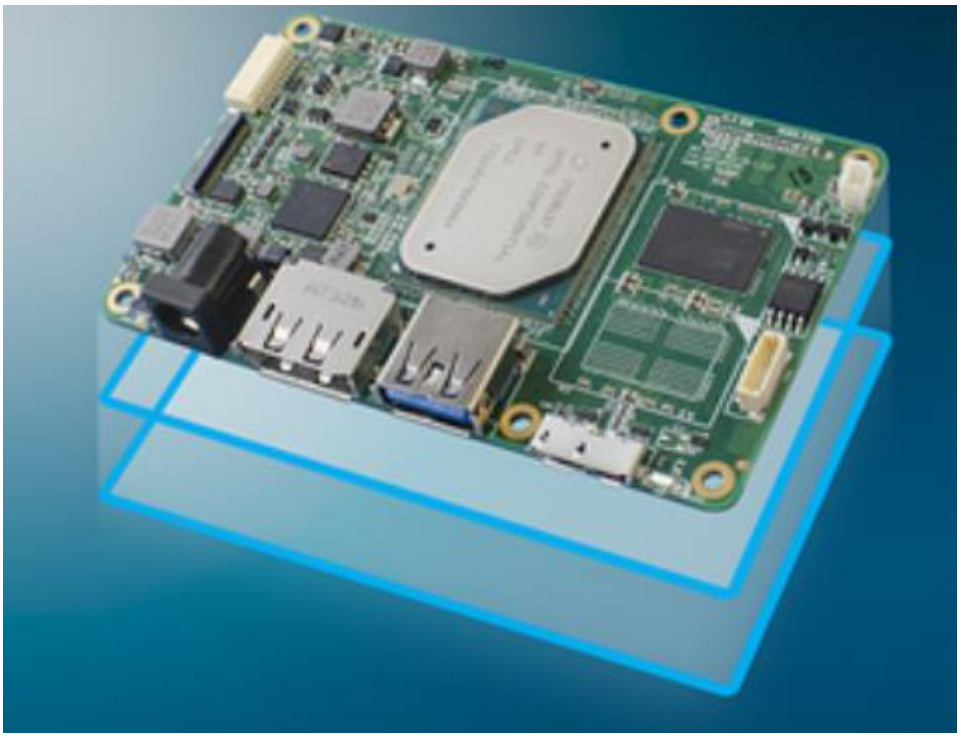
UP CORE PLUS Carrier Board Design Guide



Company Profile

Established in 1992, AAEON is one of the leading designers and manufacturers of advanced industrial and embedded computing platforms today.

Committed to innovative engineering, AAEON provides integrated solutions, hardware and services for premier OEM/ODMs and system integrators worldwide. Reliable and high quality computing platforms include industrial motherboards and systems, industrial displays, rugged tablets, PC/104, PICMG and COM modules, embedded SBCs, embedded controllers, network appliances and related accessories. AAEON also offers customized end-to-end services from initial product conceptualization and product development on through to volume manufacturing and after-sales service programs.

With a continuous pursuit of innovation and excellence, AAEON became a member of the ASUS group in 2011, further strengthening its leadership fueled by advanced technology from ASUS and leveraging resources within the group. AAEON is posed to offer more diversified embedded products and solutions at higher quality standards to meet world-class design and manufacturing demands in the years to come.

AAEON is an Associate member of the Intel® Intelligent Systems Alliance.

AAEON Core Values

Reliability: Delivering trustworthy products on a timely manner to our customers

Integrity: We value business integrity and ethics, making AAEON your choice business partner

Innovation: Working abreast with industry leaders to maintain technology leadership, AAEON is able to help customers turn cutting-edge concepts into reality

Revision History

Version	Release Date	Remark
V0.1	2018/09/05	First release
V0.2	2019/03/19	
V0.3	2020/01/08	Update drawing

1.0 UP CORE PLUS Carrier board Pinout

DOCKING 1

Pin	EXPANSION CONNECTOR	Description	Plat. Power	Pwrgood Assert State
A1	5V	Power supply MB to carrier board or carrier board to MB	Voltage tolerance DC±2% , per pin 0.5A	
A2	5V	Power supply MB to carrier board or carrier board to MB	Voltage tolerance DC±2% , per pin 0.5A	
A3	5V	Power supply MB to carrier board or carrier board to MB	Voltage tolerance DC±2% , per pin 0.5A	
A4	5V	Power supply MB to carrier board or carrier board to MB	Voltage tolerance DC±2% , per pin 0.5A	
A5	5V	Power supply MB to carrier board or carrier board to MB	Voltage tolerance DC±2% , per pin 0.5A	
A6	5V	Power supply MB to carrier board or carrier board to MB	Voltage tolerance DC±2% , per pin 0.5A	
A7	5V	Power supply MB to carrier board or carrier board to MB	Voltage tolerance DC±2% , per pin 0.5A	
A8	5V	Power supply MB to carrier board or carrier board to MB	Voltage tolerance DC±2% , per pin 0.5A	
A9	GND	GND		
A10	GND	GND		
A11	PMU_ PLT_RST#	**Reset button input signal.**	+V3.3A	
A12	UART1_RTS	UART Ready to Send	+V1.8A	
A13	PMU_PWRBTN_N	**Power button input signal. Used to wake the SOC from power button press.**	+V3.3A	
A14	UART1_CTS	UART Clear to Send	+V1.8A	

A15	PMU_SLP_S3_N	Low in S3 and lower. Controls power delivery subsystem.	+V3.3A	
A16	GPIO43/UART1_TX	UART data output	+V1.8A	
A17	PCIE_CLKREQ3#	**Used for devices that need to request one of the four output clocks. Each clock request maps to the matching clock output (for example, PCI_CLKREQ[3] maps to PCIE_CLKP/N[3]). These signals are multiplexed and may be used by other functions.**	+V1.8A	**External pull up 10k ohm**
A18	GPIO42/UART1_RX	UART data input	+V1.8A	
A19	PCIE_WAKE3_N	PCIe wake signal	+V1.8A	
A20	GND	GND		
A21	GND	GND		
A22	GPIO25/CPU_prog_JTAG_TDO	GPIO available for platform use/FPGA prog JTAG TDO	+V1.8A	
A23	GPIO110/SIO_SPI_0_TXD	GPIO available for platform use/SPI Data Out	+V1.8A	
A24	GPIO24/CPU_prog_JTAG_TMS	GPIO available for platform use/FPGA prog JTAG TMS	+V1.8A	
A25	GPIO109/SIO_SPI_0_RXD	GPIO available for platform use/SPI Data In	+V1.8A	
A26	HDMI_CEC_D	For HDMI CEC control : GPIO20 => CPU_GPIO_CEC_IN	+V1.8A	

		GPIO21 => CPU_GPIO_CEC_OUT		
A27	GPIO104/SIO_SPI_0_CLK	GPIO available for platform use/ SPI Clock	+V1.8A	
A28	GPIO23/CPU_prog_JTAG_TCK	GPIO available for platform use/ FPGA prog JTAG TCK	+V1.8A	
A29	GPIO105/SIO_SPI_0_FS0	GPIO available for platform use/ SPI Slave Select	+V1.8A	
A30	GPIO22/CPU_prog_JTAG_TDI	GPIO available for platform use/ FPGA prog JTAG TDI	+V1.8A	
A31	GPIO106/SIO_SPI_0_FS1	GPIO available for platform use/ SPI Slave Select	+V1.8A	
A32	ISH_GPIO0	GPIO for wake, interrupt, alert, etc., from sensors	+V1.8A	
A33	GND	GND		
A34	ISH_GPIO_1	GPIO for wake, interrupt, alert, etc., from sensors	+V1.8A	
A35	LPC_AD0	LPC Multiplexed Command, Address, Data bit [0]	+V1.8A	
A36	ISH_GPIO2	GPIO for wake, interrupt, alert, etc., from sensors	+V1.8A	
A37	LPC_R_AD1	LPC Multiplexed Command, Address, Data bit [1]	+V1.8A	
A38	ISH_GPIO3	GPIO for wake, interrupt, alert, etc., from sensors	+V1.8A	
A39	LPC_R_AD2	LPC Multiplexed Command, Address, Data bit [2]	+V1.8A	

A40	ISH_GPIO_4	GPIO for wake, interrupt, alert, etc., from sensors	+V1.8A	
A41	LPC_R_AD3	LPC Multiplexed Command, Address, Data bit [3]	+V1.8A	
A42	ISH_GPIO_5	GPIO for wake, interrupt, alert, etc., from sensors	+V1.8A	
A43	GND	GND		
A44	ISH_GPIO_6	GPIO for wake, interrupt, alert, etc., from sensors	+V1.8A	
A45	GPIO84/AVS_I2S2_MCLK	GPIO available for platform use/ MCLK for Master Mode operation or GPIO. Should be Fs*256 or 19.2 MHz. May be unused in slave mode. *optional signal*	+V1.8A	
A46	GPIO34/PWM0	Pulse Width Modulator for control of vibra motors, backlight display, etc.	+V1.8A	
A47	GPIO86/AVS_I2S2_WS_SYNC	GPIO available for platform use/ Audio Codec frame synchronization or Word select signal. Bidirectional – may be configured for master or slave	+V1.8A	
A48	GPIO35/PWM1	Pulse Width Modulator for control of vibra motors, backlight display, etc.	+V1.8A	
A49	GPIO87/AVS_I2S2_SDI	GPIO available for platform use/Audio Codec I2S Data in – serial data shifted in	+V1.8A	
A50	GND	GND		

A51	GPIO88/AVS_I2S2_SDO	GPIO available for platform use/Audio Codec I2S Data out – serial data shifted out	+V1.8A	
A52	GPIO136/I2C_SDA6	GPIO available for platform use/I2C data signal	+V1.8A	
A53	GND	GND		
A54	GPIO137/I2C_SCL6	GPIO available for platform use/I2C clock signal	+V1.8A	
A55	PCIE_P5_USB3_P2_TXP	PCIE EXPRESS transmit / USB 3.0 transmit	+V1.24A	
A56	GND	GND		
A57	PCIE_P5_USB3_P2_TXN	PCIE EXPRESS transmit / USB 3.0 transmit	+V1.24A	
A58	GPIO85/AVS_I2S2_BCLK	GPIO available for platform use/Audio Codec I2S Bit Clock – bidirectional. In master mode, the BCLK is supplied by the SoC. In slave mode, serves as an input.	+V1.8A	
A59	GND	GND		
A60	GPIO18/BT_HOST_WAKE	GPIO available for platform use/Blue tooth host wake signal	+V1.8A	
A61	PCIE_P5_USB3_P2_RXP	PCIE EXPRESS receive / USB 3.0 receive		
A62	GND	GND		
A63	PCIE_P5_USB3_P2_RXN	PCIE EXPRESS receive / USB 3.0 receive	+V1.24A	
A64	USB2_DP2	Universal serial bus port differential pairs	+V3.3A	

A65	GND	GND		
A66	USB2_DN2	Universal serial bus port differential pairs	+V3.3A	
A67	PCIE_REFCLK3_P	PCIE REFERENCE CLOCK differential pairs	+V1.24A	
A68	GND	GND		
A69	PCIE_REFCLK3_N	PCIE REFERENCE CLOCK differential pairs	+V1.24A	
A70	GPIO218/nSTATUS	GPIO available for platform use/ FPGA nSTATUS	+V1.8A	
A71	GND	GND		
A72	GND	GND		
A73	GPIO124/I2C_SDA0	GPIO available for platform use/I2C data signal	+V1.8A	
A74	ISH_GPIO_7	GPIO for wake, interrupt, alert, etc., from sensors	+V1.8A	
A75	GPIO125/I2C_SCL0	GPIO available for platform use/ I2C clock signal	+V1.8A	
A76	ISH_GPIO_8	GPIO for wake, interrupt, alert, etc., from sensors	+V1.8A	
A77	GND	GND		
A78	ISH_GPIO_9	GPIO for wake, interrupt, alert, etc., from sensors	+V1.8A	
A79	GPIO126/I2C_SDA1	GPIO available for platform use/I2C data signal	V1P8	
A80	ISH_GPIO_10	GPIO for wake, interrupt, alert, etc., from sensors	V1P8	

A81	GPIO127/I2C_SCL1	GPIO available for platform use/ I2C clock signal	+V1.8A	
A82	ISH_GPIO_11	GPIO for wake, interrupt, alert, etc., from sensors	+V1.8A	
A83	GND	GND		
A84	ISH_GPIO_12	GPIO for wake, interrupt, alert, etc., from sensors	+V1.8A	
A85	GPIO_2	GPIO available for platform use	+V1.8A	
A86	ISH_GPIO_13	GPIO for wake, interrupt, alert, etc., from sensors	+V1.8A	
A87	GPIO_3	GPIO available for platform use	+V1.8A	
A88	ISH_GPIO_14	GPIO for wake, interrupt, alert, etc., from sensors	+V1.8A	
A89	GND	GND		
A90	PMIC_IRQ_N	PMIC IRQ N	+V1.8A	
A91	LPC_FRAME_N	LFRAME# indicates the start of an LPC cycle, or an abort.	+V1.8A	
A92	GPIO5/FPGA_CLR	GPIO available for platform use/ FPFA clear signal	+V1.8A	
A93	LPC_CLKOUT0	LPC clock signal	+V1.8A	
A94	GND	GND		
A95	LPC_CLKRUN_N	Control LPC Clock Signals	+V1.8A	
A96	GPIO217/FPGA_OE	GPIO available for platform use/ FPFA OE signal	+V1.8A	
A97	LPC_SERIRQ	Serial Interrupt Request	+V1.8A	

A98	GPIO216/FPGA_RST	GPIO available for platform use/ FPFA RESET signal	+V1.8A	
A99	GPIO19/CONFIG_SEL	GPIO available for platform use/ FPFA config selection signal	+V1.8A	
A100	GPIO27/FPGA_fw_re-load	GPIO available for platform use/ FPFA firmware re-load signal	+V1.8A	

DOCKING 2

Pin	EXPANSION CONNECTOR	Description	Plat. Power	Pwrgood Assert State
B1	12V	Power supply MB to carrier board or carrier board to MB	Voltage tolerance DC±2% , per pin 0.5A	
B2	12V	Power supply MB to carrier board or carrier board to MB	Voltage tolerance DC±2% , per pin 0.5A	
B3	12V	Power supply MB to carrier board or carrier board to MB	Voltage tolerance DC±2% , per pin 0.5A	
B4	12V	Power supply MB to carrier board or carrier board to MB	Voltage tolerance DC±2% , per pin 0.5A	
B5	12V	Power supply MB to carrier board or carrier board to MB	Voltage tolerance DC±2% , per pin 0.5A	
B6	12V	Power supply MB to carrier board or carrier board to MB	Voltage tolerance DC±2% , per pin 0.5A	

B7	12V	Power supply MB to carrier board or carrier board to MB	Voltage tolerance DC±2% , per pin 0.5A	
B8	12V	Power supply MB to carrier board or carrier board to MB	Voltage tolerance DC±2% , per pin 0.5A	
B9	NC	NC		
B10	NC	NC		
B11	DDI0_HPD	Hot plug detect input	+V1.8A	
B12	GND	GND		
B13	DDI0_TXP_1	Transmit serial data output differential pairs	+V1.05A	
B14	DDI0_TXP_0	Transmit serial data output differential pairs	+V1.05A	
B15	DDI0_TXN_1	Transmit serial data output differential pairs	+V1.05A	
B16	DDI0_TXN_0	Transmit serial data output differential pairs	+V1.05A	
B17	GND	GND		
B18	GND	GND		
B19	DDI0_TXP_2	Transmit serial data output differential pairs	+V1.05A	
B20	DDI0_TXP_3	Transmit serial data output differential pairs	+V1.05A	
B21	DDI0_TXN_2	Transmit serial data output differential pairs	+V1.05A	
B22	DDI0_TXN_3	Transmit serial data output differential pairs	+V1.05A	
B23	GND	GND		

B24	GND	GND		
B25	DDI0_AUXP	Aux port for Display port	+V1.05A	
B26	DDI0_DDCCLK	Display I2C interface	+V1.8A	
B27	DDI0_AUXN	Aux port for Display port	+V1.05A	
B28	DDI0_DDCDATA	Display I2C interface	+V1.8A	
B29	GND	GND		
B30	GND	GND		
B31	PCIE_REFCLK0_P	PCIE REFERENCE CLOCK differential pairs	+V1.24A	
B32	PCIE_REFCLK1_P	PCIE REFERENCE CLOCK differential pairs	+V1.24A	
B33	PCIE_REFCLK0_N	PCIE REFERENCE CLOCK differential pairs	+V1.24A	
B34	PCIE_REFCLK1_N	PCIE REFERENCE CLOCK differential pairs	+V1.24A	
B35	GND	GND		
B36	GND	GND		
B37	PCIE_RXP0	PCIE EXPRESS receive	+V1.24A	
B38	PCIE_RXP1	PCIE EXPRESS receive	+V1.24A	
B39	PCIE_RXN0	PCIE EXPRESS receive	+V1.24A	
B40	PCIE_RXN1	PCIE EXPRESS receive	+V1.24A	
B41	GND	GND		
B42	GND	GND		
B43	PCIE_TXP0	PCIE EXPRESS transmit	+V1.24A	

B44	PCIE_TXP1	PCIE EXPRESS transmit	+V1.24A	
B45	PCIE_TXN0	PCIE EXPRESS transmit	+V1.24A	
B46	PCIE_TXN1	PCIE EXPRESS transmit	+V1.24A	
B47	GND	GND		
B48	GND	GND		
B49	PCIE_REFCLK2_P	PCIE REFERENCE CLOCK differential pairs	+V1.24A	
B50	PCIE_P3_USB3_P4_TXP	PCIE EXPRESS transmit / USB 3.0 transmit	+V1.24A	
B51	PCIE_REFCLK2_N	PCIE REFERENCE CLOCK differential pairs	+V1.24A	
B52	PCIE_P3_USB3_P4_TXN	PCIE EXPRESS transmit / USB 3.0 transmit	+V1.24A	
B53	GND	GND		
B54	GND	GND		
B55	PCIE_TXP2	PCIE EXPRESS transmit	+V1.24A	
B56	PCIE_P3_USB3_P4_RXP	PCIE EXPRESS receive / USB 3.0 receive	+V1.24A	
B57	PCIE_TXN2	PCIE EXPRESS transmit	+V1.24A	
B58	PCIE_P3_USB3_P4_RXN	PCIE EXPRESS receive / USB 3.0 receive	+V1.24A	
B59	GND	GND		
B60	GND	GND		
B61	PCIE_RXP2	PCIE EXPRESS receive	+V1.24A	
B62	SATA_P1_USB3_P5_RXN	SATA receive / USB 3.0 receive	+V1.24A	

B63	PCIE_RXN2	PCIE EXPRESS receive	+V1.24A	
B64	SATA_P1_USB3_P5_RXP	SATA receive / USB 3.0 receive	+V1.24A	
B65	GND	GND		
B66	GND	GND		
B67	PCIE_P4_USB3_P3_TXP	PCIE EXPRESS transmit / USB 3.0 transmit	+V1.24A	
B68	SATA_P1_USB3_P5_TXN	SATA transmit / USB 3.0 transmit	+V1.24A	
B69	PCIE_P4_USB3_P3_TXN	PCIE EXPRESS transmit / USB 3.0 transmit	+V1.24A	
B70	SATA_P1_USB3_P5_TXP	PCIE EXPRESS transmit / USB 3.0 transmit	+V1.24A	
B71	GND	GND		
B72	GND	GND		
B73	PCIE_P4_USB3_P3_RXP	PCIE EXPRESS receive / USB 3.0 receive	+V1.24A	
B74	SATA_RXN0	SATA receive	+V1.24A	
B75	PCIE_P4_USB3_P3_RXN	PCIE EXPRESS receive / USB 3.0 receive	+V1.24A	
B76	SATA_RXP0	SATA receive	+V1.24A	
B77	GND	GND		
B78	GND	GND		
B79	USB2_DP3	Universal serial bus port differential pairs	+V3.3A	
B80	SATA_TXP0	SATA transmit	+V1.24A	

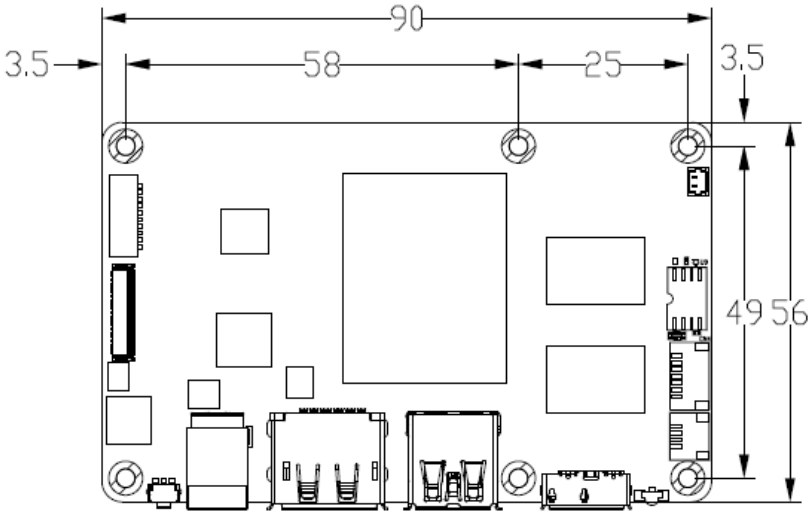
B81	USB2_DN3	Universal serial bus port differential pairs	+V3.3A	
B82	SATA_TXN0	SATA transmit	+V1.24A	
B83	GND	GND		
B84	GND	GND		
B85	USB2_DP4	Universal serial bus port differential pairs	+V3.3A	
B86	USB2_DP5	Universal serial bus port differential pairs	+V3.3A	
B87	USB2_DN4	Universal serial bus port differential pairs	+V3.3A	
B88	USB2_DN5	Universal serial bus port differential pairs	+V3.3A	
B89	GND	GND		
B90	GND	GND		
B91	PWRON_PNLVDDEN	Panel power enable	+V1.8A	
B92	GPIO26/SATA_LED_N	GPIO available for platform use/SATA LED	+V1.8A	
B93	PLTRST/PNLBKLEN	Platform reset/Panel backlight brightness control	+V1.8A	
B94	DDI0_BKLTCTL	Panel backlight brightness control	+V1.8A	
B95	PCIE_WAKE0_N	PCIE WAKE signal	+V1.8A	
B96	PCIE_CLKREQ0#	PCIE CLOCK REQUEST	+V1.8A	External pull up 10k ohm

B97	PCIE_WAKE1_N	PCIE WAKE signal	+V1.8A	
B98	PCIE_CLKREQ1#	PCIE CLOCK REQUEST	+V1.8A	External pull up 10k ohm
B99	PCIE_WAKE2_N	PCIE WAKE signal	+V1.8A	
B100	PCIE_CLKREQ2#	PCIE CLOCK REQUEST	+V1.8A	External pull up 10k ohm

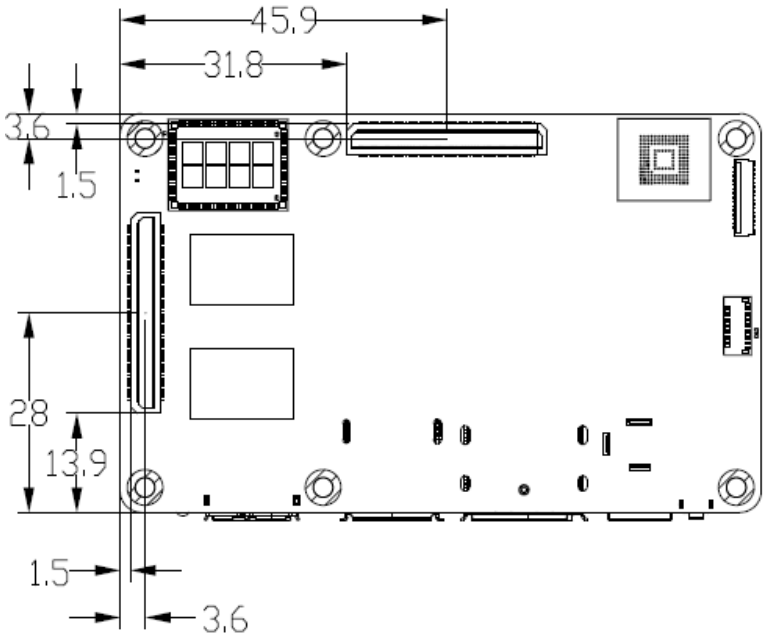
2.0 UP CORE PLUS Mechanical Specification

2.1 UP CORE PLUS Module Form Factors

TOP SIDE:



BOTTOM SIDE:



Side of the board

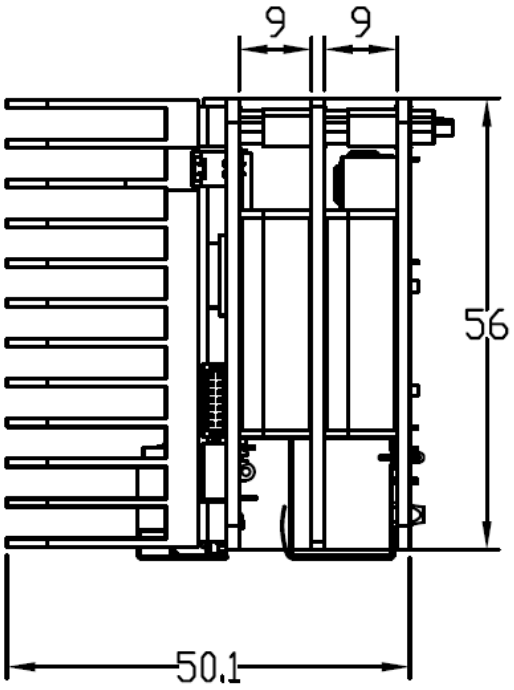


Figure 2-1 Module Form Factors

Figure 2-1 AAEON UP CORE Module

2.2 UP CORE PLUS Carrier Board Connectors

UP CORE PLUS M/B module utilizes two 100-pin high density connectors to interface the UP CORE plus module and carrier board. To design Carrier Board Connector:

Connector Socket type : PANASONIC / AXK5S00347YG

Mated Height : 9 mm

AXK(5(S)/6(S))

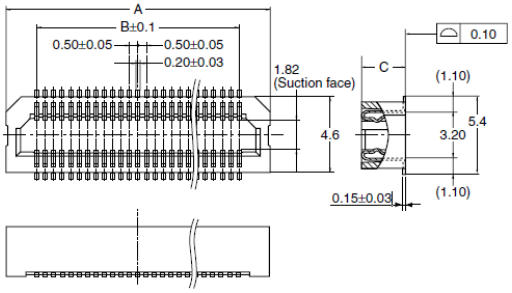
P5KS: Mated height 4.0mm, 4.5mm, 5.0mm, 5.5mm, 6.0mm, 6.5mm, 7.0mm, 8.0mm, 9.0mm type

• Socket

CAD Data

Dimension table (mm)

No. of pins	A	B
20	8.20	4.50
24	9.20	5.50
30	10.70	7.00
34	11.70	8.00
36	12.20	8.50
40	13.20	9.50
50	15.70	12.00
60	18.20	14.50
70	20.70	17.00
80	23.20	19.50
100	28.20	24.50



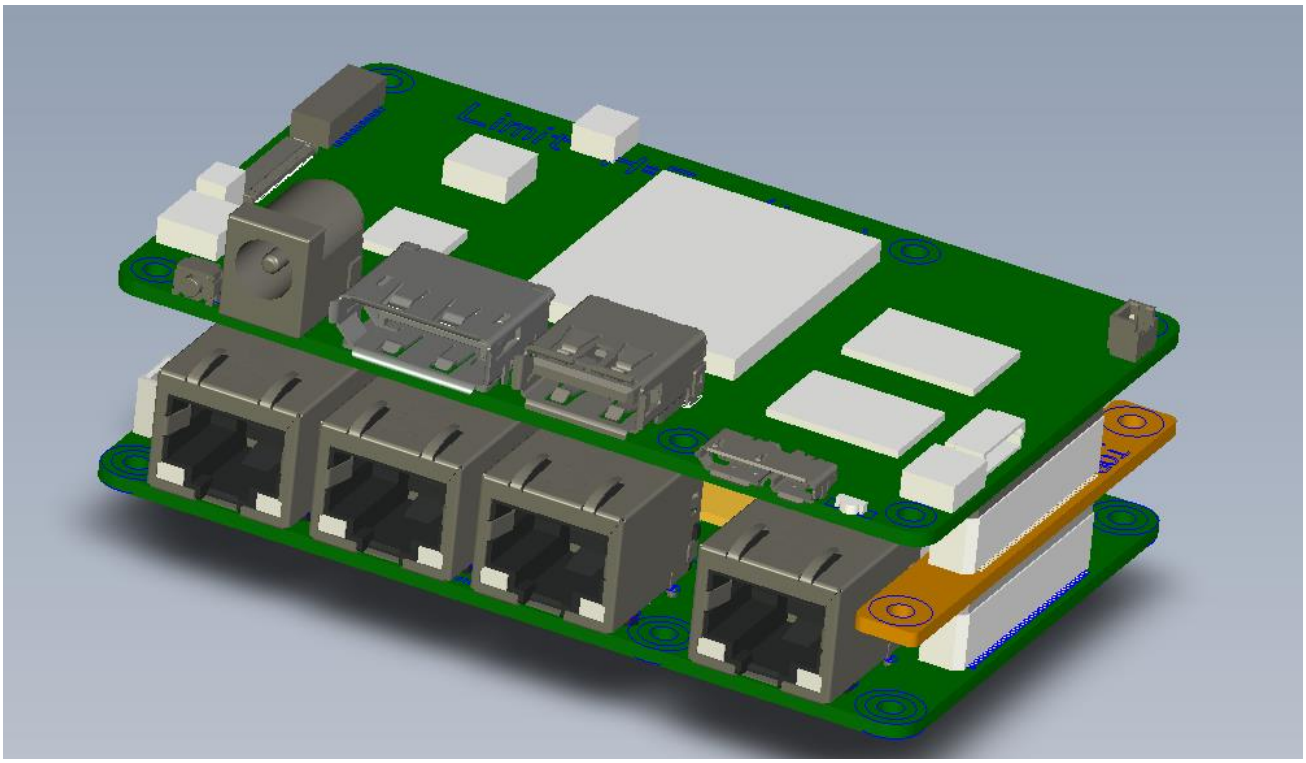
General tolerance: ±0.2

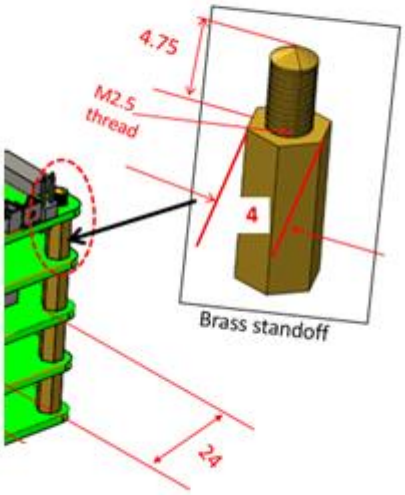
Mated height	C
4.0 mm, 5.0 mm, 6.0 mm	3.05
4.5 mm, 5.5 mm, 6.5 mm	3.55
7.0 mm, 8.0 mm, 9.0 mm	6.05

Figure 2-2-1 Carrier Board Connector

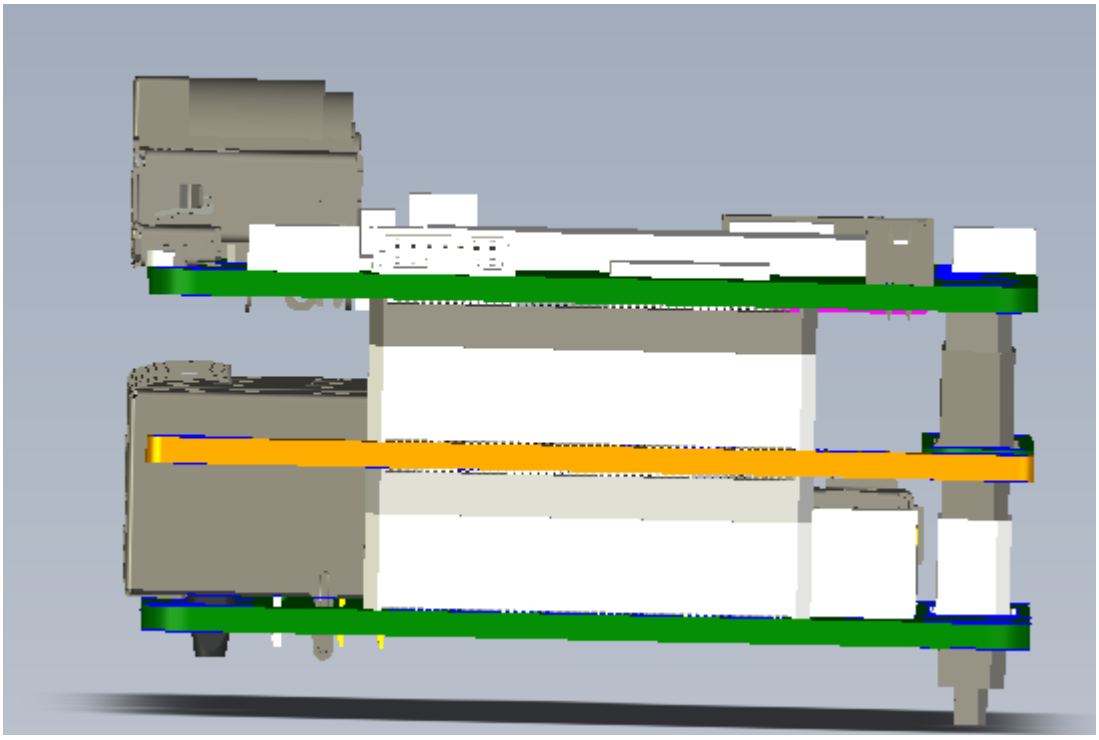
2.3 PCB dimension reference

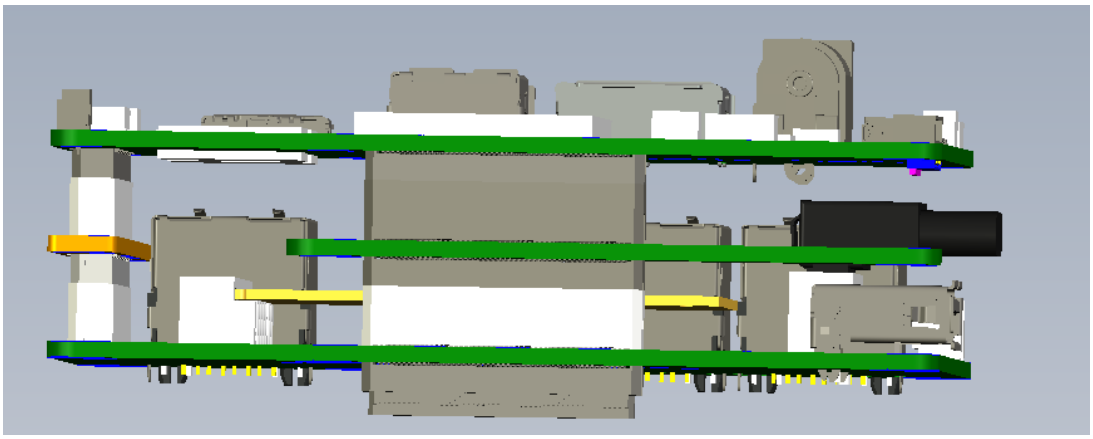
2.3.1 UP CORE plus system reference





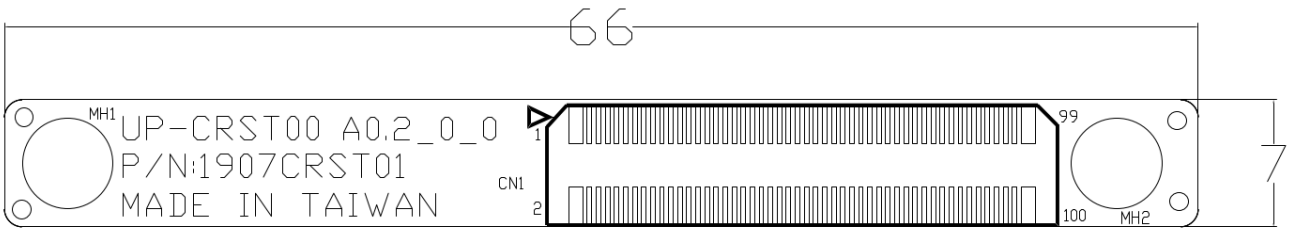
2.3.2 UP CORE PLUS MB

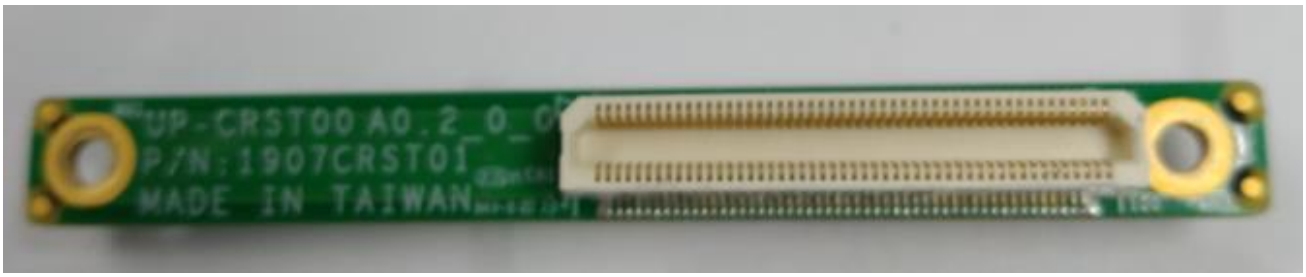




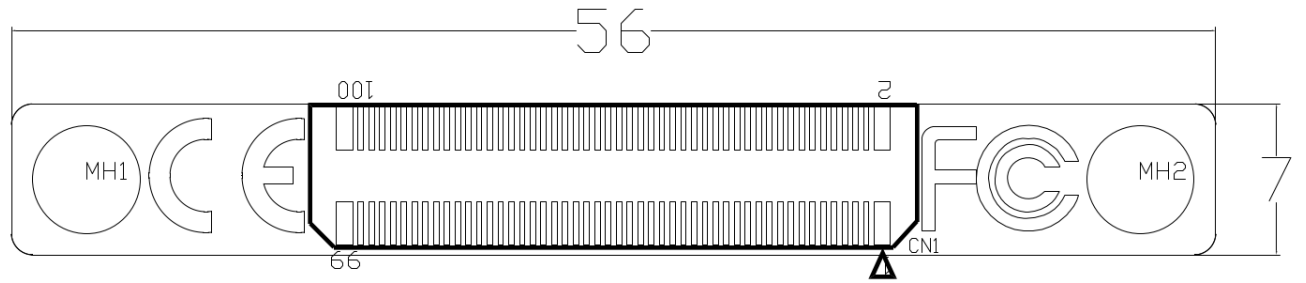
2.3.3 Spacer Carrier board

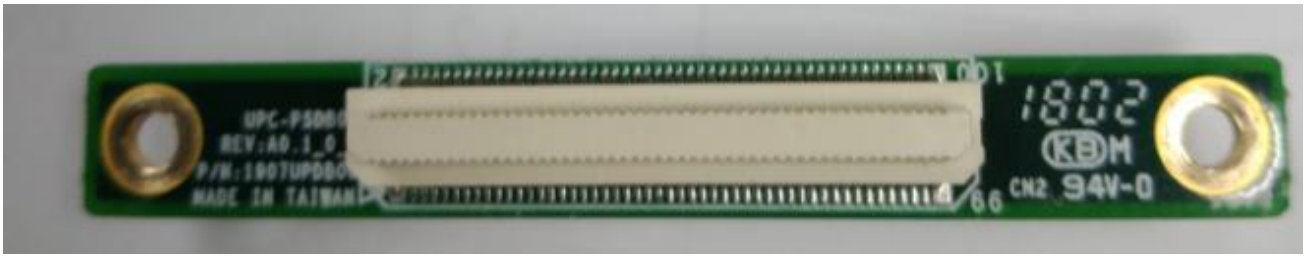
Docking 1





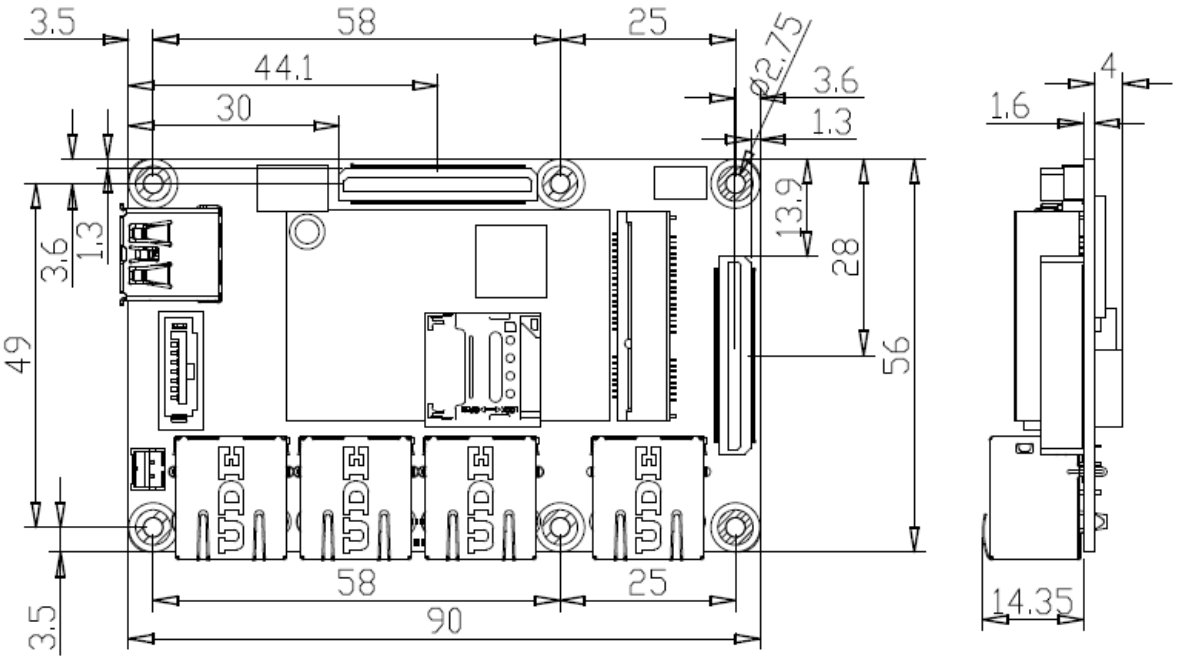
Docking 2



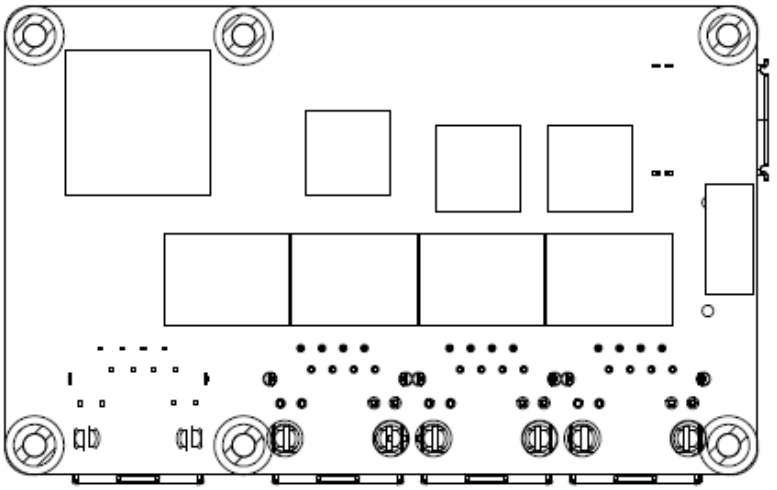


2.3.4 Carrier board (user customize)

TOP SIDE:



BOTTOM SIDE



3.0 PCB STACK

3.1 PCB Stack Example

Layer	Stack up	Material	Thickness (mil)	Reference	Single End			Differentail		
					40 Ω ±15%	42 Ω ±10%	50 Ω ±10%	68 Ω ±10%	85 Ω ±10%	100 Ω ±10%
	SM	Soldermask	0.8							
1	TOP	0.5 oz+Platting	1.7	L2	7.5	6.5	4.5	7/4/7	4.5/5/4.5	4/12/4
		1080HR	2.82							
2	GND1	1 oz	1.3							
		Core	3							
3	IN1	1 oz	1.3	L2,L5	5.5	5	3.5	6/4/6	3.5/4.5/3.5	3.5/20/3.5
		2116HR	4.5							
4	IN2	1 oz	1.3	L2,L5	5.5	5	3.5	6/4/6	3.5/4.5/3.5	3.5/20/3.5
		Core	3							
5	GND2	1 oz	1.3							
		2116HR	2.84							
6	IN3	1 oz	1.3	L5,L8	6	5.5	3.5	6/4/6	3.5/4.5/3.5	3.5/12/3.5
		Core	12							
7	IN4	1 oz	1.3	L5,L8	6	5.5	3.5	6/4/6	3.5/4.5/3.5	3.5/12/3.5
		2116HR	2.84							
8	VCC	1 oz	1.3							
		Core	3							
9	IN5	1 oz	1.3	L8,L11	5.5	5	3.5	6/4/6	3.5/4.5/3.5	3.5/20/3.5
		2116HR	4.5							
10	IN6	1 oz	1.3	L8,L11	5.5	5	3.5	6/4/6	3.5/4.5/3.5	3.5/20/3.5
		Core	3							
11	GND3	1 oz	1.3							
		1080HR	2.82							
12	BOT	0.5 oz+Platting	1.7	L11	7.5	6.5	4.5	7/4/7	4.5/5/4.5	4/12/4
	SM	Soldermask	0.8							
Total Thickness			62.32							

Design should follow above impedance value

3.2 Main routing general layout requirement

Table 3. Single-ended Transmission Line Specifications

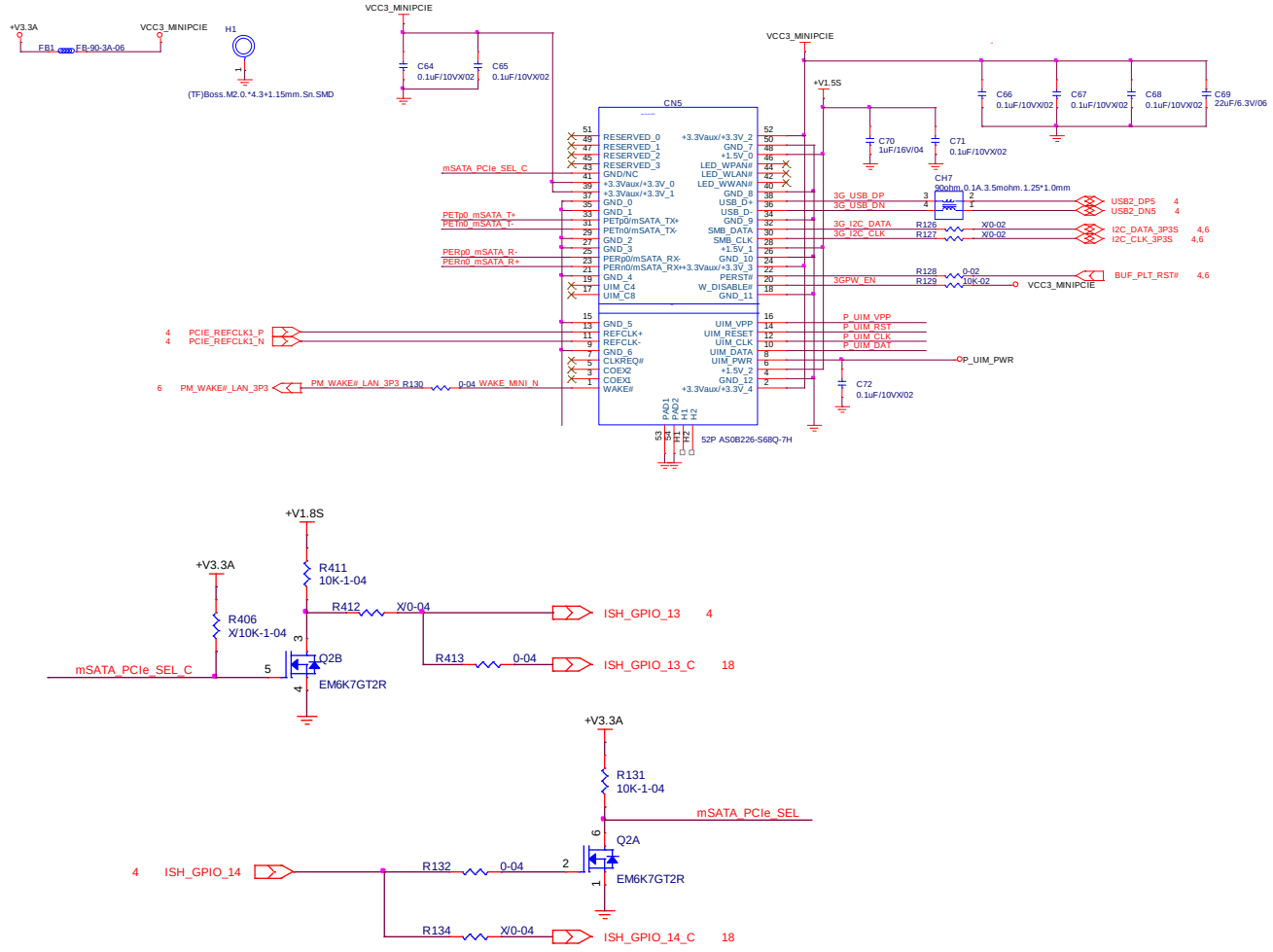
Interface	Breakout/Break-in PCB Routing		Main PCB Route Target Impedance 50Ω			
			Microstrip 50Ω ± 15%		Dual Stripline 50Ω ± 10%	
	Width /Min Spacing	Max Routing Length (mils / mm)	Trace Width (mils / mm)	Min Trace Spacing (mils / mm)	Trace Width (mils / mm)	Min Trace Spacing (mils / mm)
SD Card	3.5/3.5 (mils)	500 / 12.7	4 / 0.102	Data - 8/ 0.203 CLK - 15 / 0.381	4.5 / 0.114	Data - 8/ 0.203 CLK - 15 / 0.381
eMMC	3.5/3.5 (mils)	300 / 7.62	4 / 0.102	Data - 10/ 0.254 CLK - 15 / 0.381	4.5 / 0.114	Data - 10/ 0.254 CLK - 15 / 0.381
JTAG	3.5/3.5 (mils)	500 / 12.7	4 / 0.102	5 / 0.127 CLK - 12 / 0.305	4.5 / 0.114	5 / 0.127 CLK - 13.5 / 0.343
Crystal Oscillator (19.2MHz)	3.5/8 (mils)	500 / 12.7	4 / 0.102	15 / 0.382	4.5 / 0.114	15 / 0.382
RTC (32.768kHz)	3.5/4 (mils)	500 / 12.7	4 / 0.102	15 / 0.382	4.5 / 0.114	15 / 0.382
GPIOs	3.5/3.5 (mils)	500 / 12.7	4 / 0.102	5 / 0.127	4.5 / 0.114	5 / 0.127
OSC_CLK_OUT	3.5/3.5 (mils)	500 / 12.7	4 / 0.102	15 / 0.382	4.5 / 0.114	15 / 0.382
LPC	3.5/3.5 (mils)	500 / 12.7	4 / 0.102	Data - 8 / 0.203 CLK - 15 / 0.381	4.5 / 0.114	Data - 8 / 0.203 CLK - 15 / 0.381
HD Audio/DMIC	3.5/3.5 (mils)	500 / 12.7	4 / 0.102	Data - 5 / 0.127 CLK - 15 / 0.382	4.5 / 0.114	Data - 5 / 0.127 CLK - 15 / 0.381
I^2C/DDC	3.5/3.5 (mils)	500 / 12.7	4 / 0.102	Data - 5 / 0.127 CLK - 15 / 0.382	4.5 / 0.114	Data - 5 / 0.127 CLK - 15 / 0.382
SMBus	3.5/3.5 (mils)	500 / 12.7	4 / 0.102	Data - 5 / 0.127 CLK - 15 / 0.382	4.5 / 0.114	Data - 5 / 0.127 CLK - 15 / 0.382
SVID	3.5/3.5 (mils)	400 / 10.2	4 / 0.102	Data - 5 / 0.127 CLK - 15 / 0.382	4.5 / 0.114	Data - 5 / 0.127 CLK - 15 / 0.382
I2S	3.5/3.5 (mils)	500 / 12.7	4 / 0.102	Data - 5 / 0.127 CLK - 15 / 0.381	4.5 / 0.114	Data - 5 / 0.127 CLK - 15 / 0.381
UART	3.5/3.5 (mils)	500 / 12.7	4 / 0.102	5 / 0.127	4.5 / 0.114	5 / 0.127
Fast SPI	3.5/3.5 (mils)	300 / 7.62	4 / 0.102	Data - 5 / 0.127 CLK - 15 / 0.381	4.5 / 0.114	Data - 5 / 0.127 CLK - 15 / 0.381
SPI	3.5/3.5 (mils)	500 / 12.7	4 / 0.102	Data - 5 / 0.127 CLK - 15 / 0.382	4.5 / 0.114	Data - 5 / 0.127 CLK - 15 / 0.381

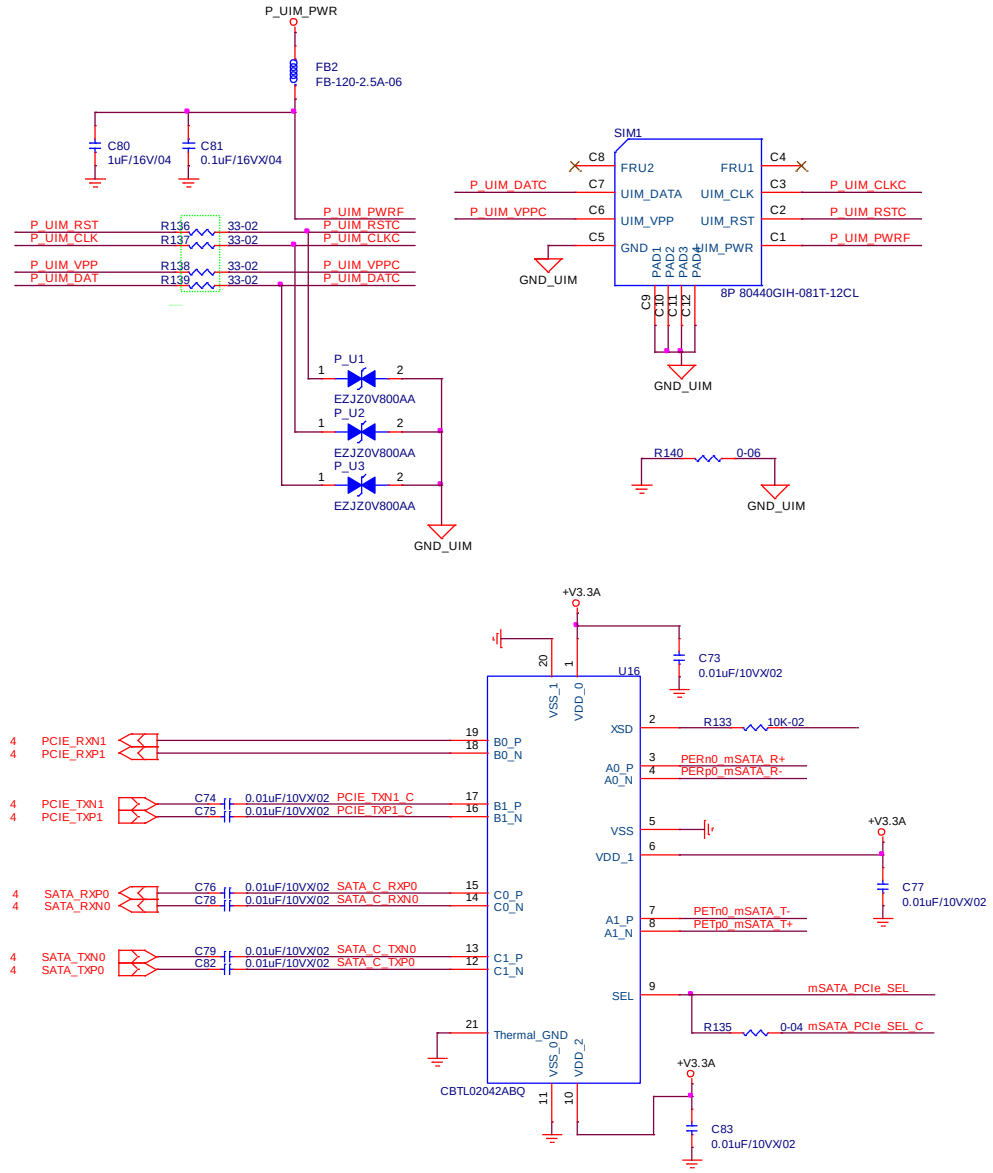
Table 4. Differential Impedance Transmission Line Specifications - Breakout Geometries

I/O Interfaces	Trace Width (mils/mm)	Trace Spacing (mils/mm)	Max Breakout Length (mils/ mm)	Minimum Pair-to -Equivalent Pair Spacing 1 (mils/ mm)	Minimum Pair-to-Non Equivalent Pair Spacing 1 (mils/mm)
HDMI	3.5 / 0.89	3.5 / 0.89	500 / 12.7	6 / 0.152	6 / 0.152
Display Port	3.5 / 0.89	3.5 / 0.89	500 / 12.7	6 / 0.152	6 / 0.152
eDP	3.5 / 0.89	3.5 / 0.89	150 / 3.81	6 / 0.152	6 / 0.152
MIPI CSI (Camera)	3.5 / 0.89	3.5 / 0.89	650 / 16.5	6 / 0.152	6 / 0.152
MIPI DSI (Display)	3.5 / 0.89	3.5 / 0.89	650 / 16.5	6 / 0.152	6 / 0.152
USB 3.0	3.5 / 0.89	3.5 / 0.89	500 / 12.7	8 / 0.203	15 / 0.381 (DSL) 20 / 0.508 (MS)
USB 2	3.5 / 0.89	3.5 / 0.89	500 / 12.7	6 / 0.152	6 / 0.152
PCIe (non interleave BO)	3.5 / 0.89	3.5 / 0.89	500 / 12.7	8 / 0.203	8 / 0.203
SATA (non interleave BO)	3.5 / 0.89	3.5 / 0.89	500 / 12.7	8 / 0.203	8 / 0.203

4.0 Circuit Reference

4.1 PCIE Mini-Card Reference Schematics





mini_XSD	mSATA_PCIe_SEL	Function	Power +3.3V_MC
High	X(Don't care)	An, Bn, Cn are Hi-Z	N/A
Low	Low	PCIe (An=Bn)	+3.3V_ALW
Low	High	mSATA (An=Cn)	+3.3V

Table 3-9: Power Ratings

Power Rail	Voltage Tolerance	D0-D2, $D3_{hot}$ Power[1]		$D3_{cold}$ Power[2,1]	
		Peak (max) mA	Normal (max) mA	Peak (max) mA	Normal (max) mA
3.3Vaux	±9%	2,750	1,100	2,750 (wake enabled)	250 (wake enabled) 5 (no wake enabled)
+1.5V	±5%	500	375	N/A	N/A

Table 2. Pin 43 statuses while different devices inserted

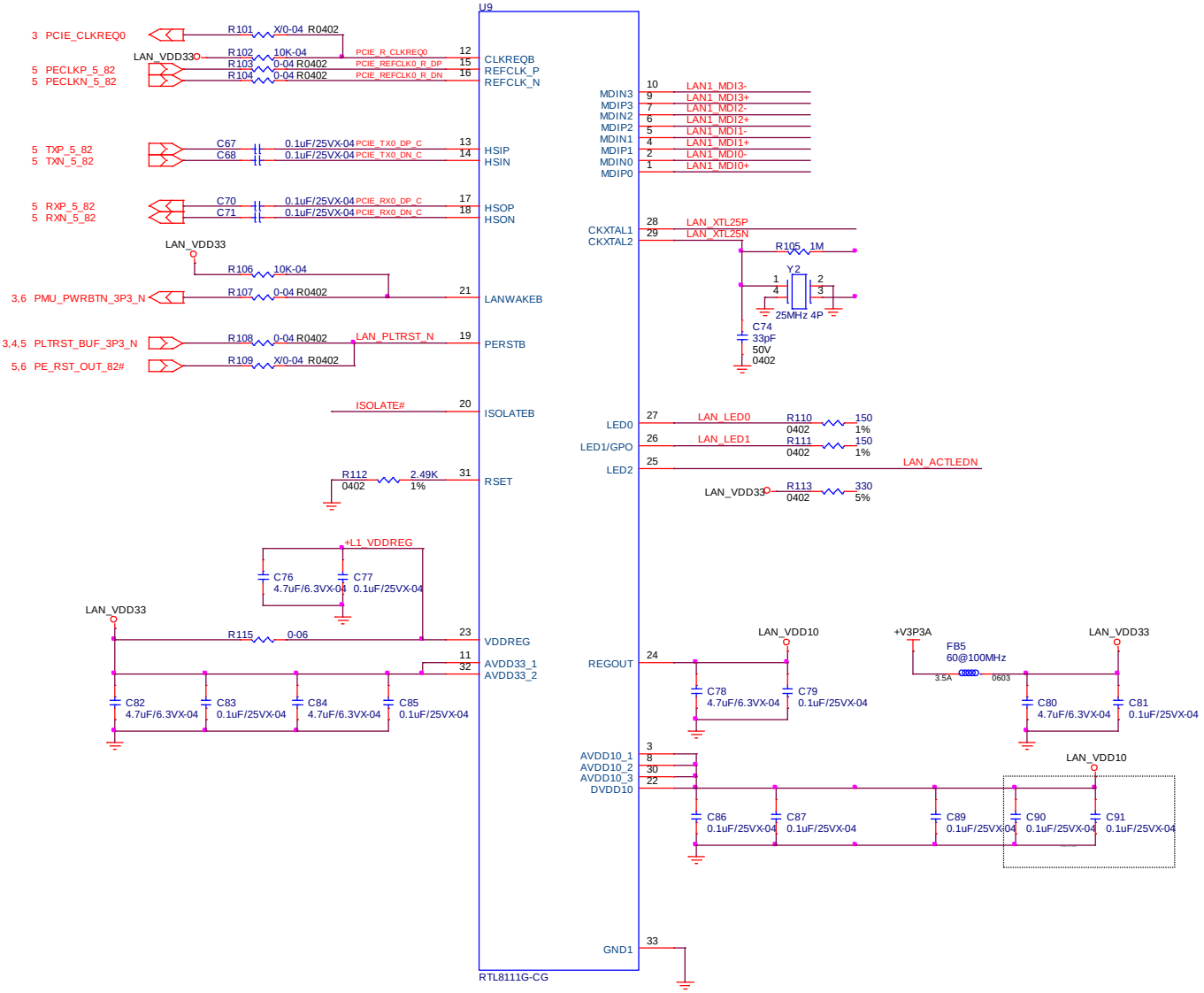
Device inserted	PCIe Mini-Card	mSATA drive
Pin 43 status	logic 0	logic 1

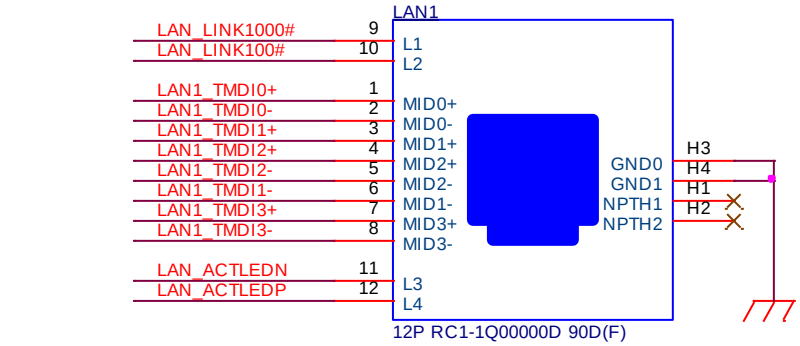
4.2 PCIE LAN Reference Schematics

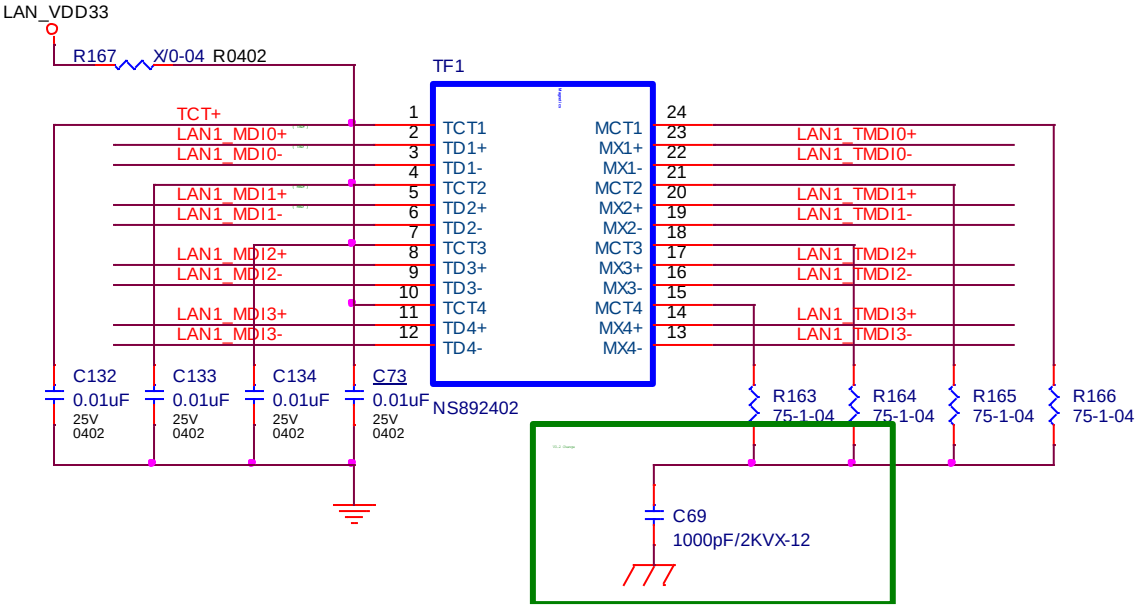
4.2.1 LAN

The 8-wire 10/100/1000BaseT Gigabit Ethernet interface compliant to the IEEE 802.3-2005 specification is the preferred interface for this port, with the carrier Module PHY responsible for implementing auto-negotiation of 10/100BaseTX vs 10/100/1000BaseT operation.

4.2.2 LAN Reference Schematics





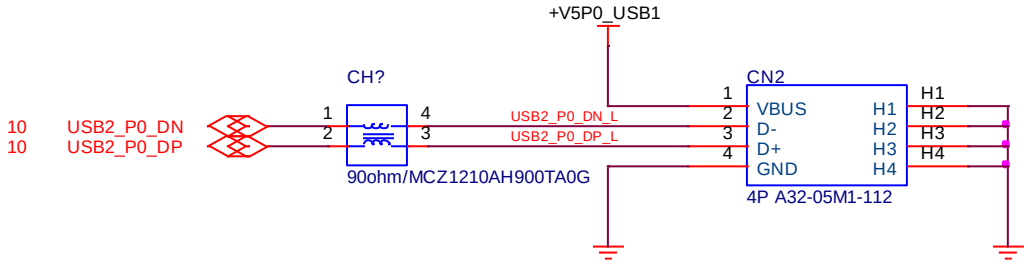


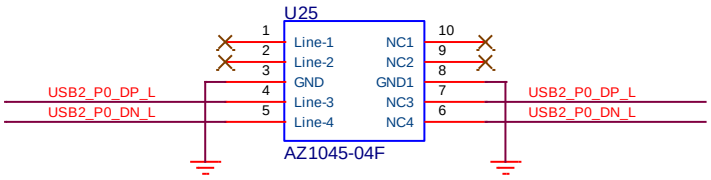
Note: TVS placement must be close to Connector for ESD Solution.

4.3 USB

All USB interfaces shall be USB 2.0 compliant. A Carrier must current limit the USB power source to minimize disruption of the Carrier in the event that a short or over-current condition exists on one of the USB Ports. A Module must fill the USB Ports starting at Port 0.

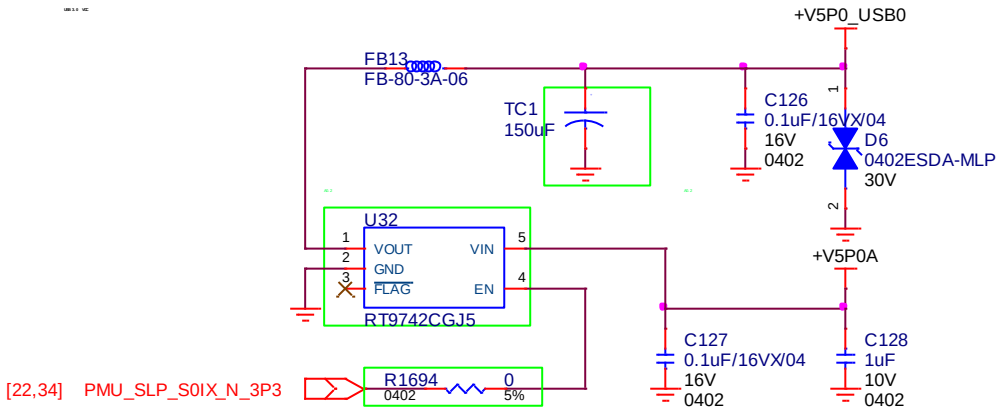
4.3.1 USB Reference Schematics - USB2.



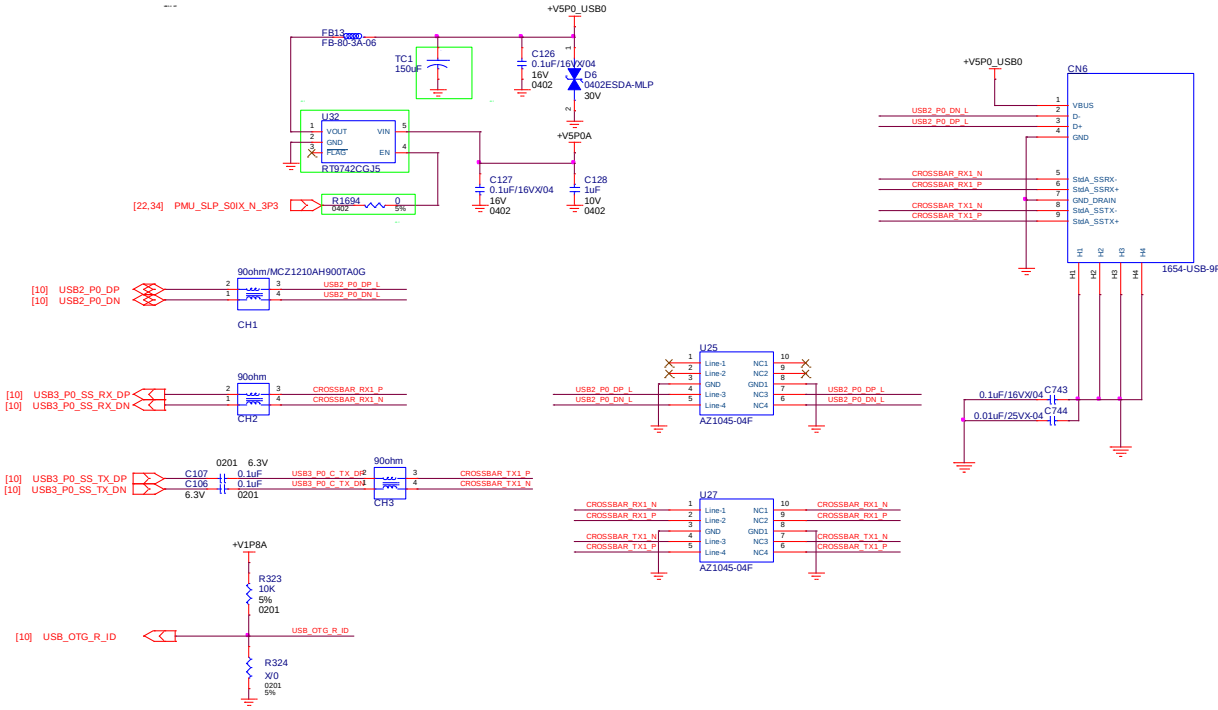


Note: TVS placement must be close to Connector for ESD Solution .

4.3.2 USB Power Over-Current Protection Reference Schematic



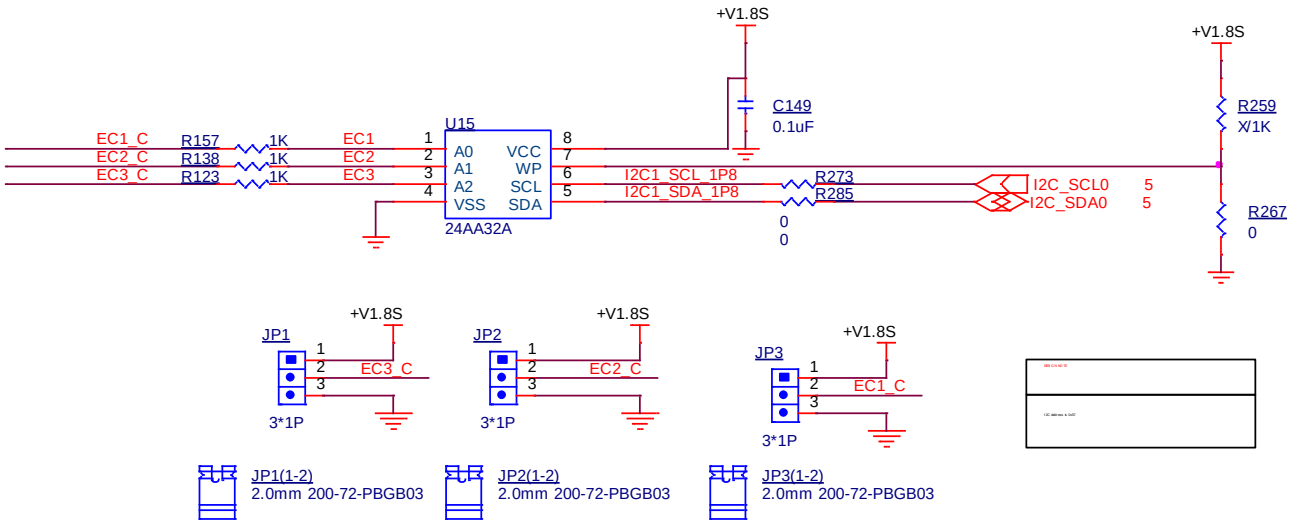
4.3.3 USB Reference Schematics – USB3.



4.4 I2C

4.4.1 I2C reference schematic

For identify Board DATA

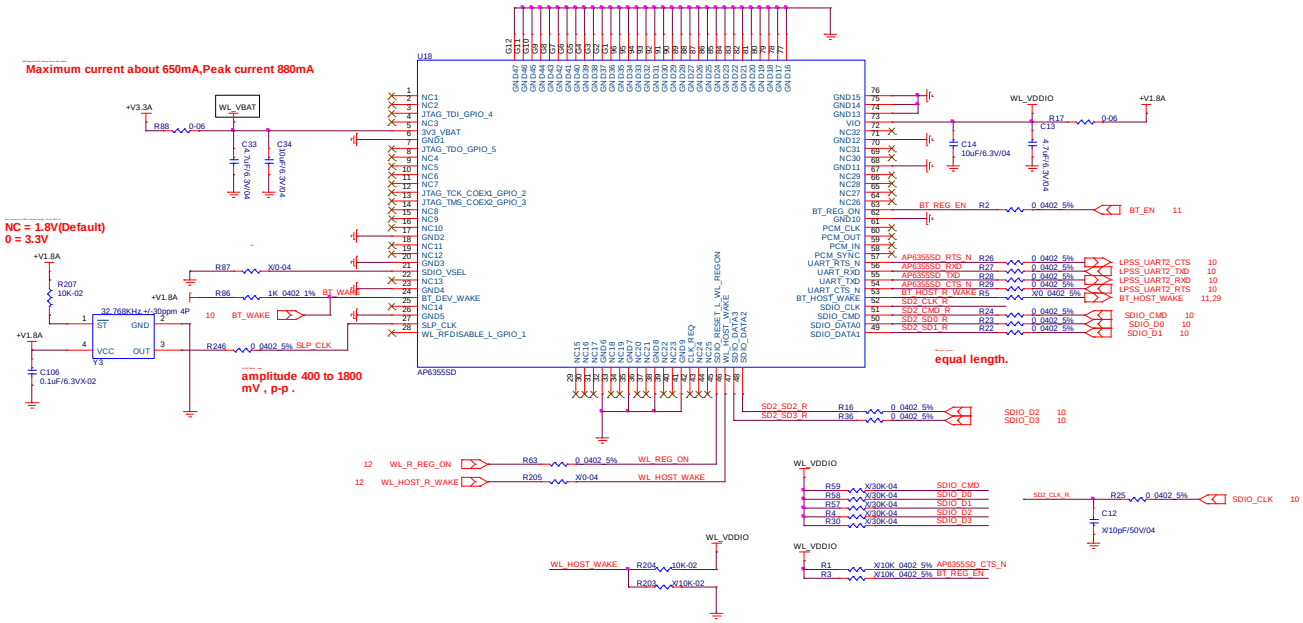


4.5 WIFI/BT_AP6355SD

The wireless module complies with IEEE 802.11 a/b/g/n/ac 1x1 antenna diversity and it can achieve up to a speed of 867Mbps with dual stream in 802.11n to connect the wireless LAN.

The integrated module provides SDIO interface for WiFi, UART / PCM interface for Bluetooth.

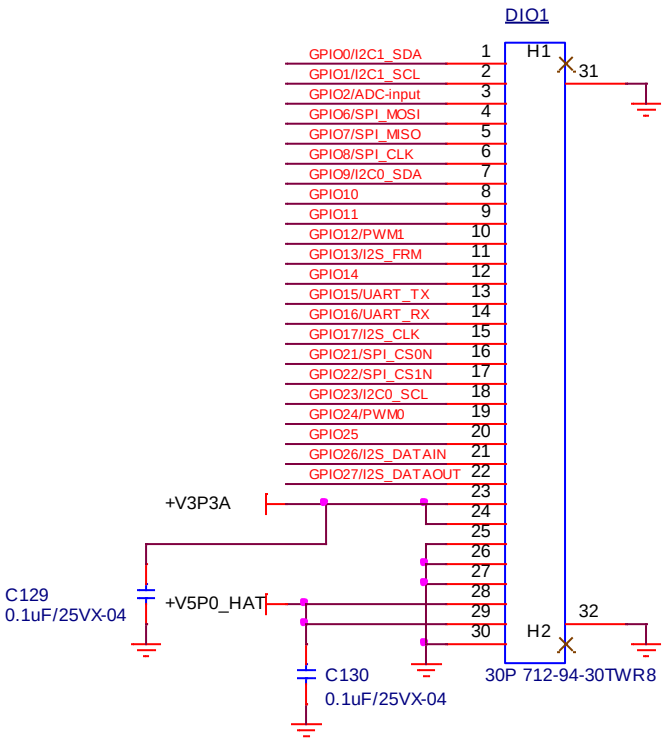
This compact module is a total solution for a combination of WiFi + BT technologies. The module is specifically developed for Smart phones and Portable devices.

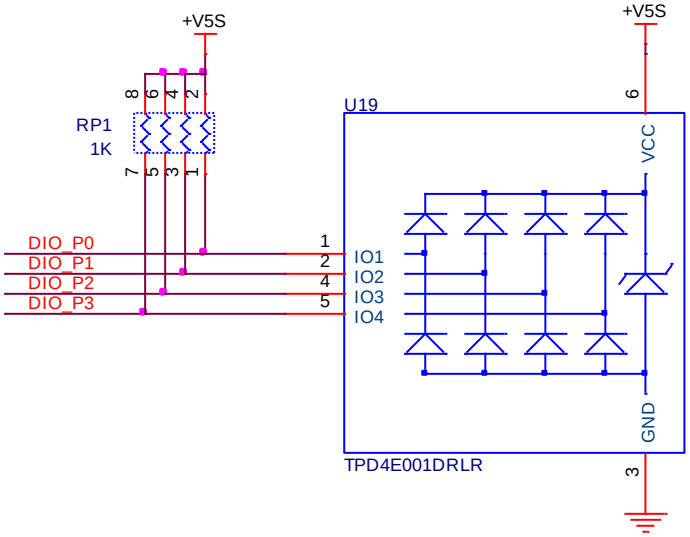


4.6 DIO

General Purpose Input / Output (GPIO)

DIO Reference Schematics

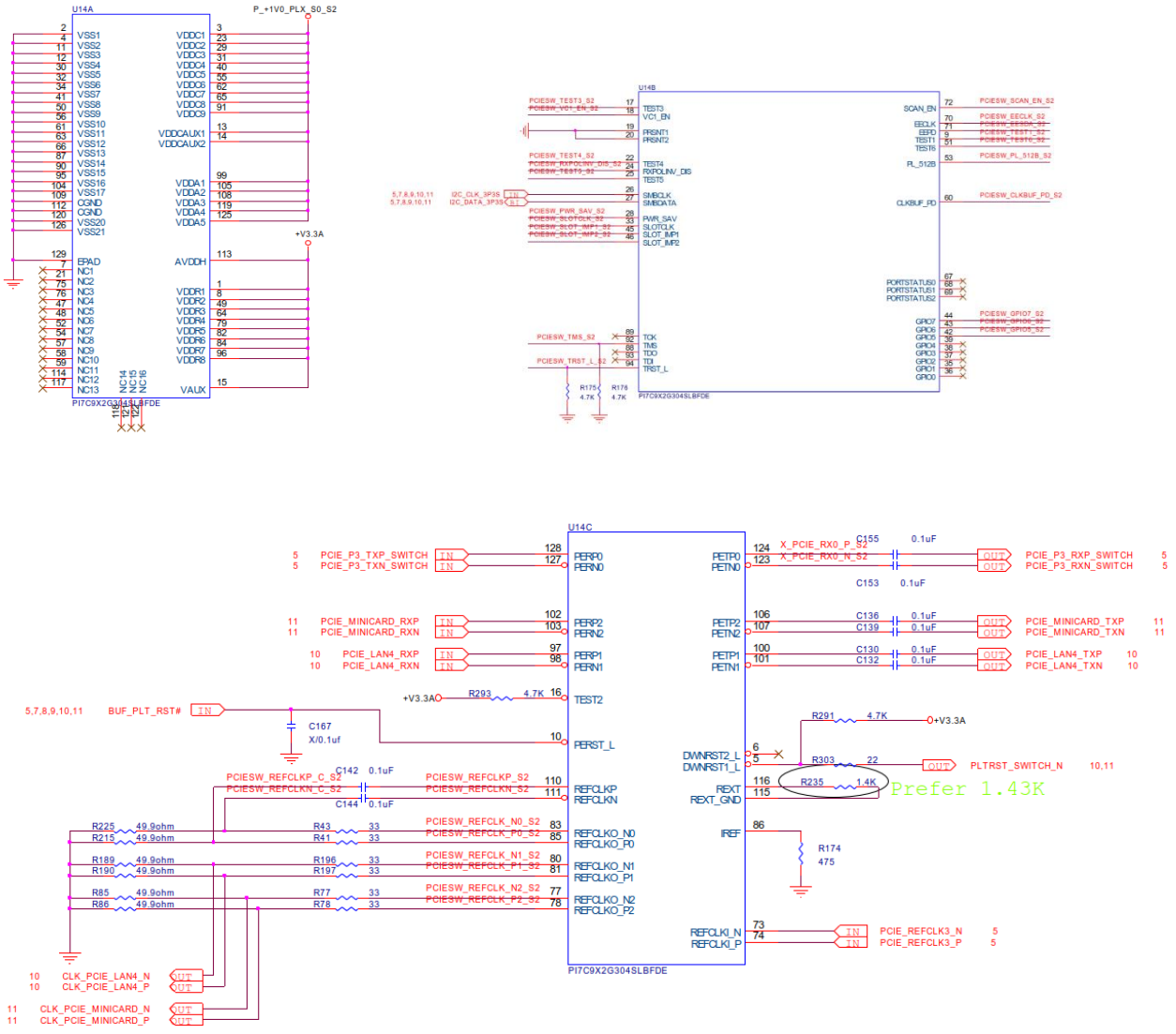




Note: (1) TVS placement must be close to Connector for ESD Solution

4.7 PCIe 2port Switch

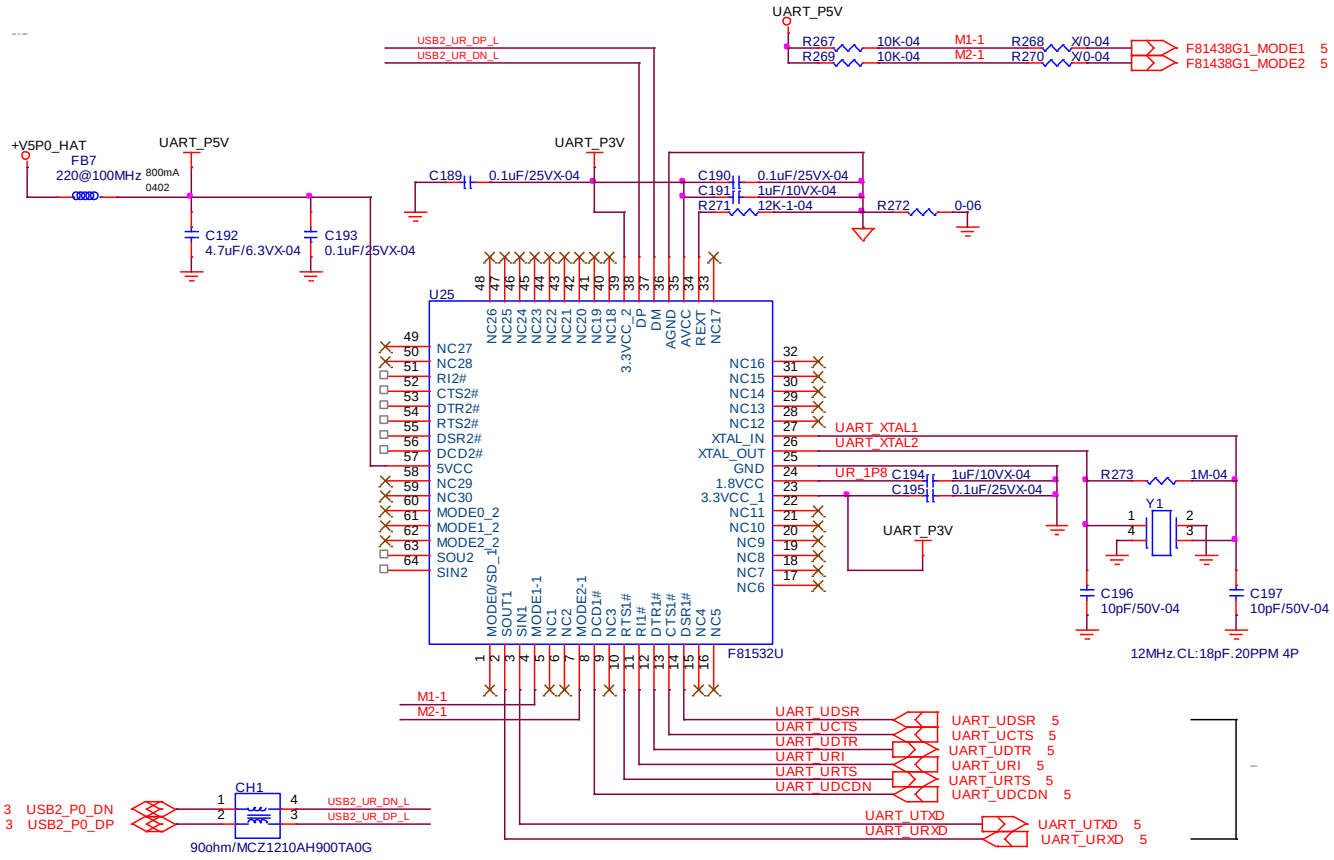
Similar to the role of PCI/PCIX Bridge in PCI/PCIX bus architecture, the function of PCI Express (PCIE) Switch is to expand the connectivity to allow more end devices to be reached by host controllers in PCIE serial interconnect architecture. The 4-lane PCIe Switch is in 3-port type configuration. It provides users the flexibility to expand or fan-out the PCI Express lanes based on their application needs.



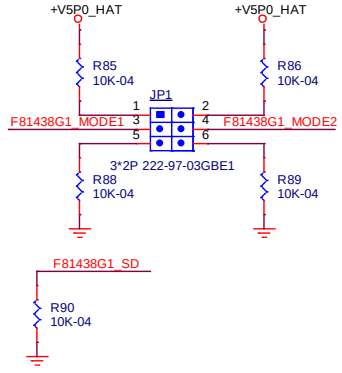
4.8 Serial Interface

Serial Interface Reference Schematic :

4.8.1 USB to UART



4.8.2 UART to RS232/422/485

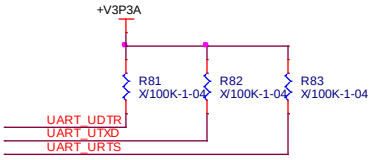


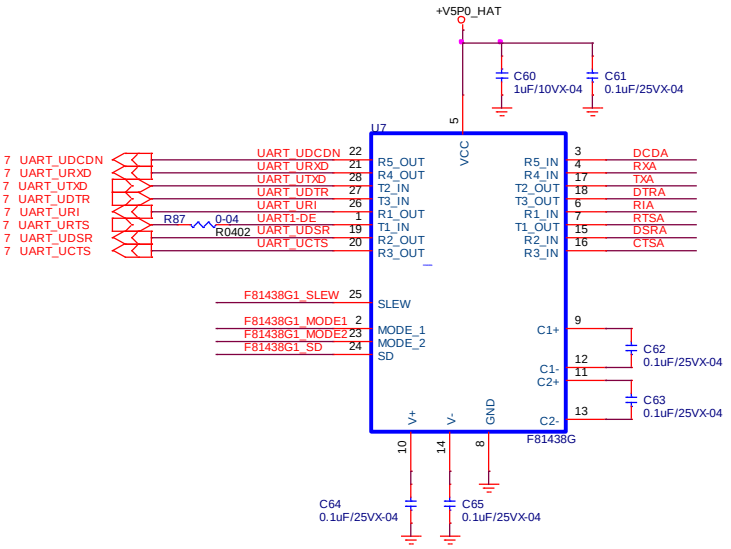
JP1(3-5)1
27S1001-0PS35-01G-R

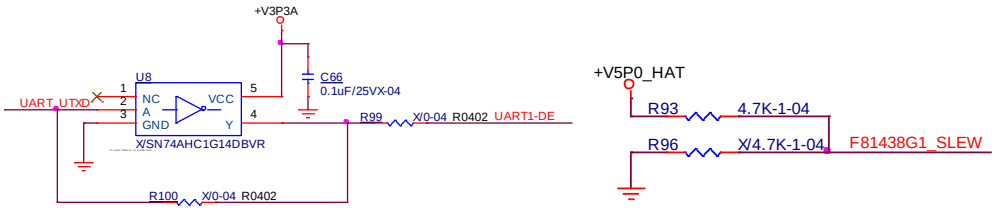
F81438G_MODE1	Selection	
1-3	1	
3-5	0	Default

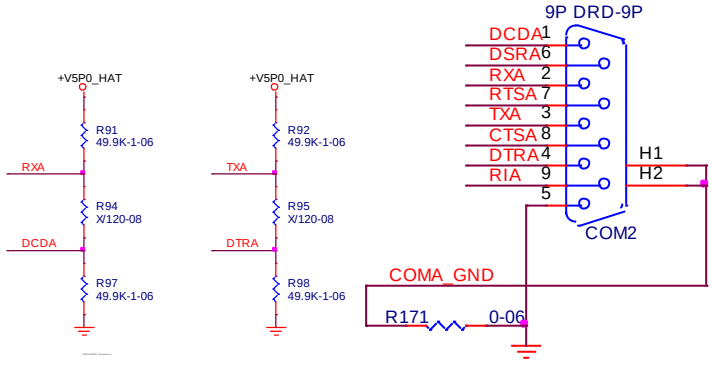
JP1(2-4)1

F81438G_MODE2	Selection	
2-4	1	Default
4-6	0	







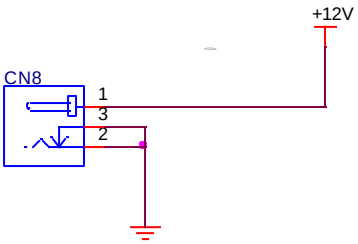


RS-232/485/422 Pin Assignment			
Pin	RS-232	RS-485	RS-422
1	DCD	RS485_D-	RS422_TX-
2	RX	RS485_D+	RS422_TX+
3	TX		RS422_RX+
4	DTR		RS422_RX-

Serlal Port Mode Selection			
SD	Mode_1	Mode_2	Mode
0	0	0	RS-422
0	0	1	RS-232 Default
0	1	1	RS-485
1	X	X	Shutdown Mode

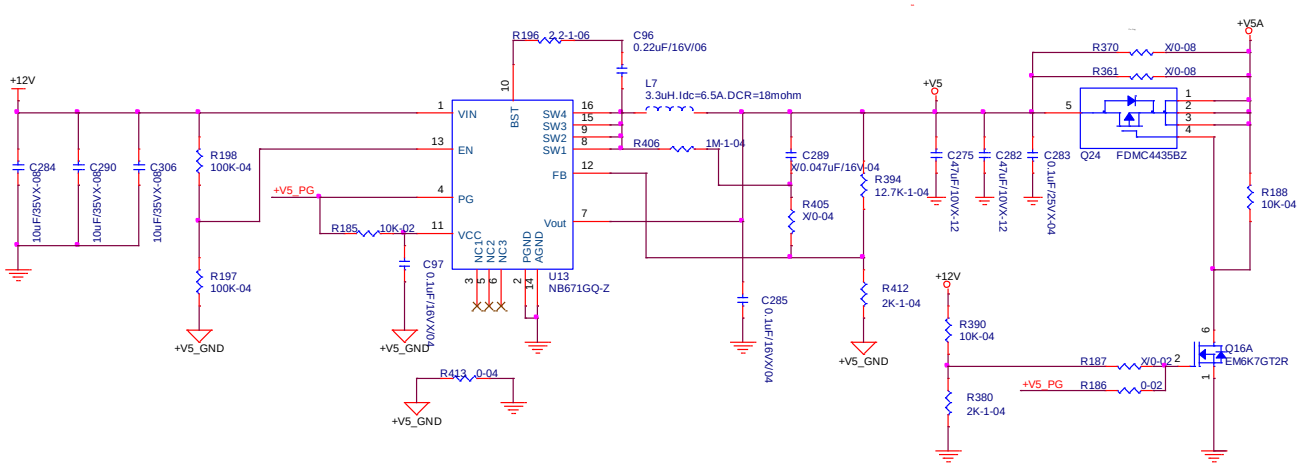
4.9 Power Management Signals

4.9.1 DC IN

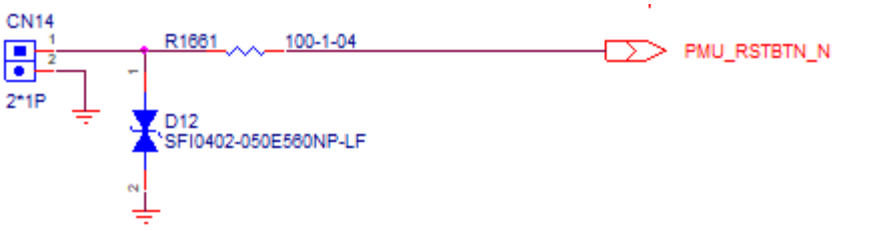


3P 416AEWTJ02004PA 90D(M)

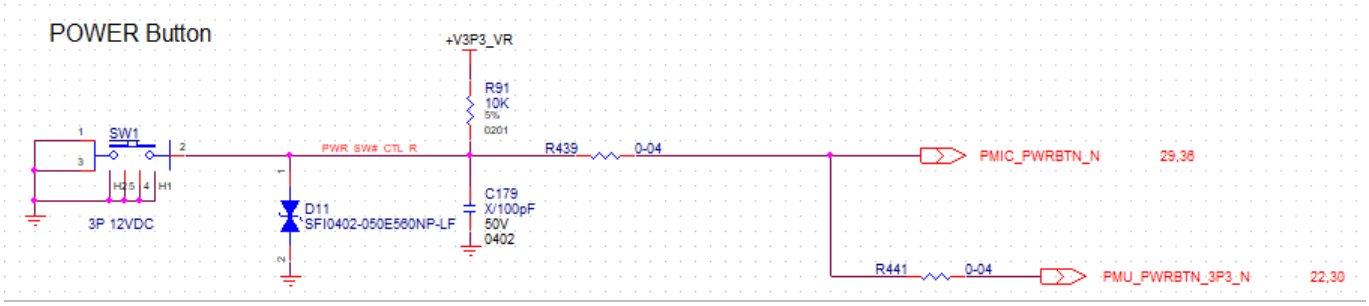
4.9.2 Voltage DC IN Protect circuit



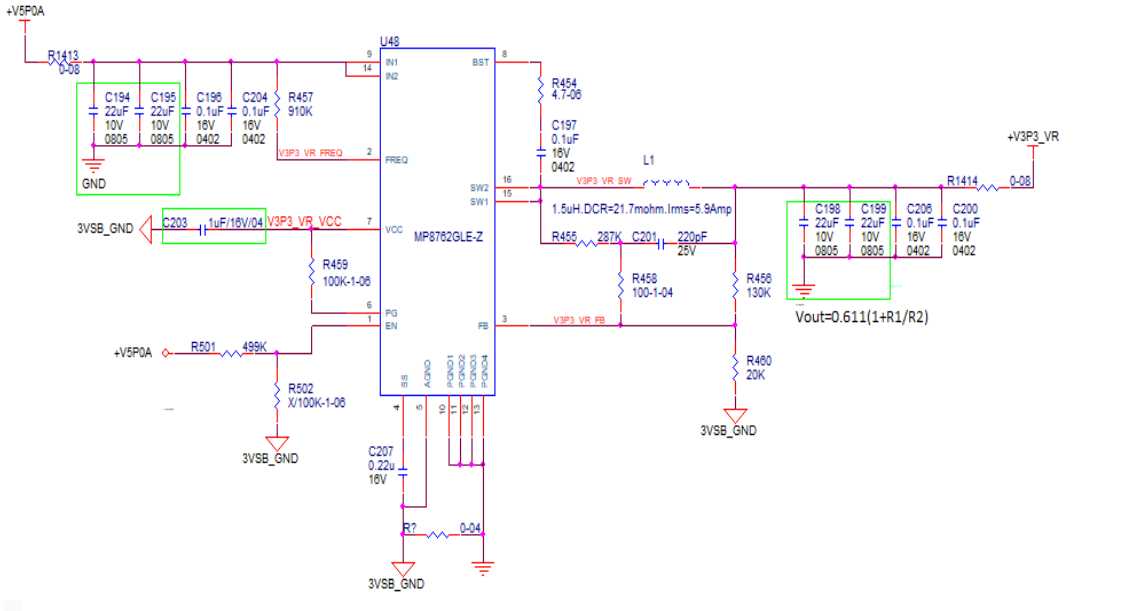
4.9.3 RESET BUTTON



4.9.4 POWER BUTTON



4.9.5 5V to 3.3V CIRCUIT



4.9.6 3.3V to 1.8V CIRCUIT